Using Dopant Activation of Implanted Wafers for Low Temperature (400°C-600°C) Measurement in CVD Equipment Design

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Abstract- We report on a method of using dopant activation Rs measurements on implanted wafers to determine actual wafer temperature and wafer heating response in order to characterize CVD chamber/heater design. We compared boron, antimony and phosphorus dopant species and found phosphorus to work best due to good amorphization of the silicon surface after implantation with complete dopant activation after 7 minutes annealing in the CVD chamber. Activation energies between 1.5 to 2.5 eV were measured over a temperature range of 420°C to 550°C for the 3 dopant species. With this technique full wafer mapping of the wafer thermal response can be obtained for designing CVD chambers/heaters.

I. Introduction

In the early stages of designing a new CVD chamber, it is critical to have an accurate method of sensing actual wafer temperature and temperature distribution/uniformity across a wafer. This information allows early heater design changes without the need to run process gases especially for temperature sensitive CVD processes. In the 450°C to 600°C temperature range one can run CVD processes which are surface reaction rate limited, where the temperature uniformity across the wafer controls the deposition rate by first order, however, there can also be gas delivery effects such as gas flow dynamics affecting deposition rate. Onishi et.al. reported on comparing B and Si+B implantation, Tsai et.al. reported on comparing BF_2 and Si+B, while Csepregi et.al. reported on comparing P, As and B [1,2,3]. Therefore, in this paper we will report on our results using solid phase epitaxial regrowth and dopant activation of amorphous layers formed by implantation at high doses (E15/cm^2) with B, Sb and P dopant species annealed in various batch and single wafer Genus CVD system designs.

II. Experimentation

Using 150mm wafers with 20nm of surface thermal oxide, the wafers were implanted with either B, Sb or P at 40keV or 100keV and 1E15 to 1E16 dose ranges to form a surface amorphous layer. These implanted wafers were then annealed in the 420°C to 550°C temperature range in the Genus 8700 batch or proto-type designs of the Genus Lynx single wafer CVD systems. The wafers were annealed in the CVD systems for 3 to 30 minutes at various temperatures ranging from 420°C to 550°C. The thermal oxides were then wet etched off and Prometrix 4-point probe resistivity (Rs) measurements were made.

III. Results

The Genus batch 8700 CVD system operates between 420°C and 460°C, while the single wafer Lynx 2 CVD system is designed to operate at 550°C. To determine dopant activation and solid phase epitaxial regrowth, Rs measurements versus annealing times were conducted and shown in Figs 1 and 2 for B and Sb implants in a batch system for 5 minute, 20 minute and 30 minute anneals. Fig 3 shows the results for P in a single wafer system (design A) at higher temperatures (550°C) and shorter times. A plot of phosphorus Rs uniformity vs. annealing time for P is shown in Fig 4. At 550°C with the P implant complete dopant activation was achieved between 5 and 7 minutes (see Fig 3) while at 460°C with either B or Sb, a 20 minute anneal was needed and at 440°C 30 minutes for Sb (see Fig 2) and over 30 minutes for B (see Fig 1).

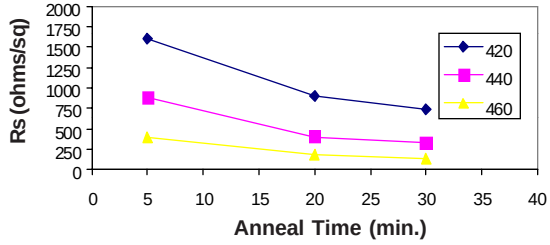

Fig 1. Boron implant annealing on Genus 8700.

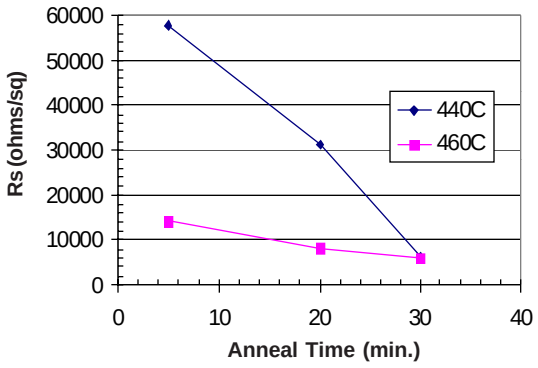

Fig 2. Sb implant annealing on Genus 8700.

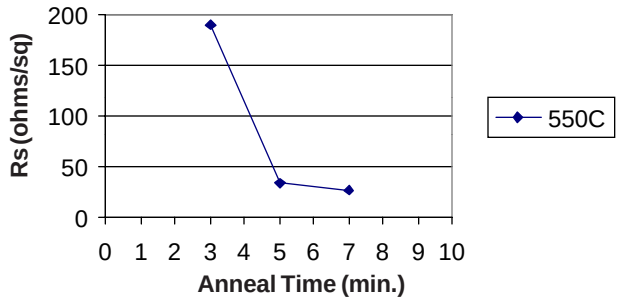

Fig 3. P implant anneal on single wafer system A.

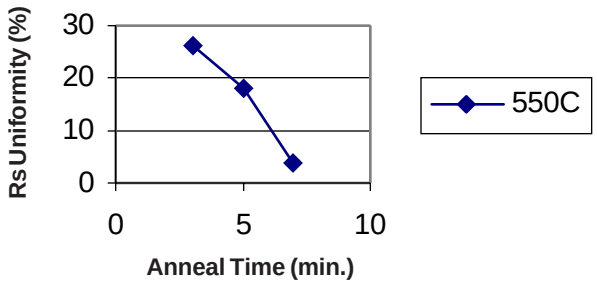

Fig 4. P implant annealing time uniformity on single wafer system design A.

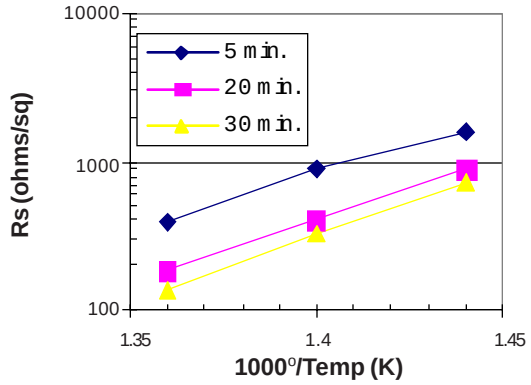

Fig 5. B implant activation energies on 8700 CVD system for 5 to 30 minutes.

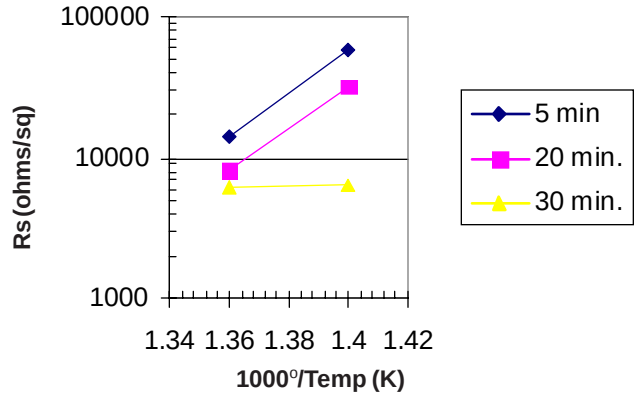

Fig 6. Sb implant activation energies on batch and single wafer system.

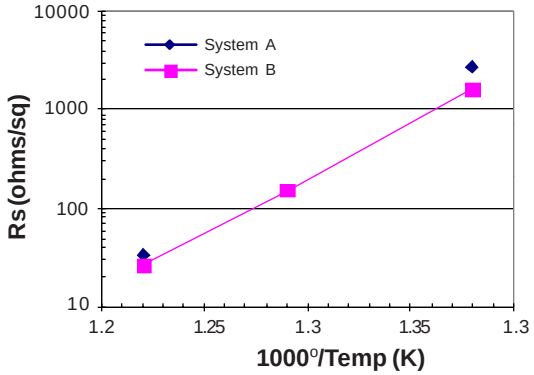

Fig 7. P implant activation energies on single wafer design A & B.

Activation energies were calculated from the arrhenius plots of Rs –vs-1/Temp. and are shown in Fig 5, 6 & 7 for B, Sb & P respectively. The activation energies for B varied from 1.51eV to 1.79eV depending on 5, 20 or 30 minute anneal time. For example 440°C anneal was 20 minutes. The minimum Rs was 306, and the maximum was 536, which corresponds to a minimum wafer temperature of 435.7°C and a maximum temperature of 448.5°C or +/-6.4°C across the wafer (+/-1.5% total temperature variation). The Sb results were 2.7eV on single wafer design B and 2.9-3.0eV on the 8700 batch system. P results were 2.5eV on single wafer design A and 2.1eV on design B. From an Rs wafer map a temperature map can be generated as shown in Figs 9 & 10 for a P implant Rs map of 522 ohms/sq. +/-22.9% and corresponding temperature wafer map of 490°C +/- 1.0%, respectively, using the prometrix software conversion [4].

This technique can also be used to determine which heater chuck in the batch 8700 CVD system is off, as illustrated in Table I where each of the 6 heater chucks were characterized. Note that heater chucks #2 was significantly cooler than the other 5 heater chucks by about 9°C.

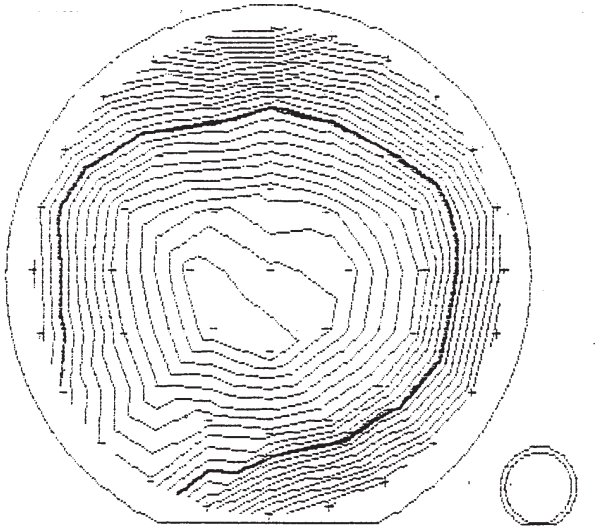

Fig 8. Prometrix Rs map of implanted wafer after 5 min. aneal at 495°C.

TABLE I.

Comparison of each of 6 wafer heater chucks in the Genus 8700 CVD System.

Chuck	Average Rs (ohm/sq)	Sigma Rs (%)	Ave. Temp. (°C)	Sigma Temp. (%)
1	1648	3.8	446	0.5
2	1937	4.8	436	0.7
3	1620	7.4	447	0.9
4	1654	6.9	445	0.9
5	1801	6.6	441	0.9
6	1727	4.7	443	0.6

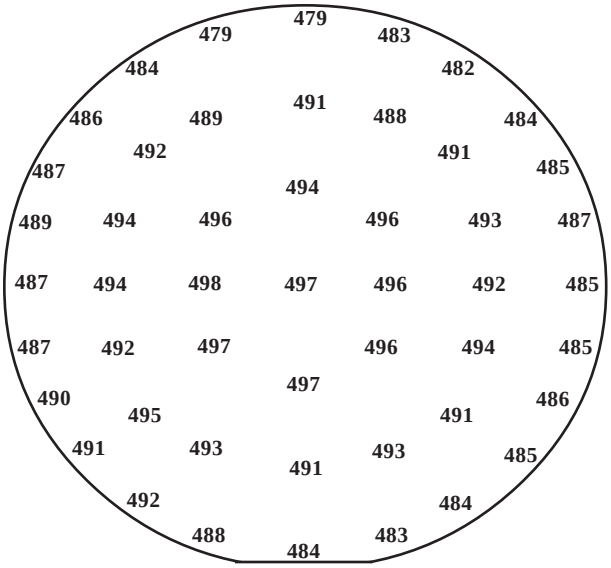

Fig 9. Calculated temperature map from Rs map above.

IV. CONCLUSION

In conclusion we have verified a method of using dopant activation of implanted wafers to characterize wafer surface temperature at low temperatures down to 420°C by using solid phase epitaxial regrowth of an implanted amorphous dopant layer. This technique has been applied to the characterization of both batch and single wafer CVD systems for temperature wafer mapping without having to use reactive gasses and resulted in shortening the development time and costs in testing new heater designs.

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