

# LOCOS –vs- Shallow Trench Isolation Latch-up Using MeV Implantation For Well Formation Down To 0.18 $\mu$ m Design Rules

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**Abstract- We report on a detailed comparative study of various MeV twin and triple well structures with either LOCOS or STI (shallow trench isolation) isolation structures for latch-up resistance for 0.35 $\mu$ m, 0.25 $\mu$ m and 0.18 $\mu$ m design rules. Diffused twin well, retrograde twin well, BL/CL (buried layer with connecting layer) twin well, BILLI (buried implant layer for lateral isolation) twin well and modified BILLI (BILLI+BL) twin well structures were all compared at various energies and doses. For LOCOS isolation structures the modified BILLI structure gave the best latch-up performance, delaying the need for STI until 0.18 $\mu$ m design rules. With STI, the modified BILLI structure also gave excellent latch-up isolation characteristics with the additional benefit of process simplification. Good defect control with excellent gate oxide integrity was achieved. The BILLI triple well structure was also found to be most desirable for triple well technology, since blanket buried layer designs cannot be used.**

## I. INTRODUCTION

Survival in the semiconductor manufacturing business is an extremely competitive economic battle. Both survival and winning in this business is closely dependent on the economic factors of *low cost semiconductor manufacturing* and showing *added value semiconductor product performance*, which can demand higher selling prices [1]. Low cost semiconductor manufacturing is achieved by: 1) net increase in sellable die per wafer and 2) process simplification through reduced processing steps. Added value semiconductor product performance can be achieved through the use of triple well structures in memory devices, and customization such as embedded/merged memory and logic devices on the same chip.

### *Increase Die/Wafer*

Three ways to increase net die per wafer are by: 1) shrinking die size through design rule scaling, 2) improving yield or minimizing yield degradation/impact by reducing new

technology introduction from previous generation design rule and 3) moving to larger diameter wafers.

### *Design Rule Scaling & Shrink*

With design rule scaling and shrinking of the minimum n<sup>+</sup> to n<sup>+</sup>, p<sup>+</sup> to p<sup>+</sup> and n<sup>+</sup> to p<sup>+</sup> spacing, maximum packing density can be achieved, netting increased die per wafer. For example, on 200mm wafers a 16Mb DRAM with 0.5 $\mu$ m design rule grosses 177die/wafer, at 0.35 $\mu$ m design rule = 650die/wafer and at 0.25 $\mu$ m design rule over 1000 die/wafer. Targeted minimum n<sup>+</sup> to p<sup>+</sup> spacing for 0.5 $\mu$ m design rule is 3.5 $\mu$ m, for 0.35 $\mu$ m design rule is 2.4 $\mu$ m, for 0.25 $\mu$ m design rule is 1.5 $\mu$ m and for 0.18 $\mu$ m design rule is 0.8 $\mu$ m. Therefore, in this paper we will report on the latch-up performance at various n<sup>+</sup> to p<sup>+</sup> spacing, for various well structures using LOCOS, modified LOCOS and STI isolation structures.

### *Extendability of Previous Generation Technology*

The majority of current generation devices use some form of modified LOCOS ie. PBL or recessed LOCOS isolation structure. Extendability of the LOCOS structure shortens the time to market of next generation products with highest possible yield, if there is no change to the process.

### *Move to Larger Diameter Wafers (300mm)*

Estimates show only a 15% economic benefit over 200mm technology, once the learning curve is mature. But this solution requires high initial capital investments, improved wafer quality and a very steep learning curve, making it high risk. It is safer and quicker to shrink and scale the device design rule.

### *Process Simplification*

The evolution from diffused well formation to MeV retrograde well can reduce process complexity by 2 mask levels with a reported cost savings of 10%. Further process simplification can be achieved through the MeV BILLI technology for a savings of upwards of 15% to 20% [2].

### Added Value Product Performance

The integration of multi-functional devices on to the same chip such as DRAM with logic, SRAM with logic or Flash with logic can be facilitated by the use of triple well designs, thereby adding value and commanding high selling prices.

## II. EXPERIMENTATION

### Isolation Formation

LOCOS isolation structures 400nm thick were formed by 1150°C oxidation, while the shallow trench isolation (STI) structures were formed by etching 400nm deep silicon trenches. This was followed by a thin, thermal oxidation to cure the etch damage at 1050°C. Use of sidewall implants to prevent side wall inversion was optional. The trenches were filled with HDP CVD oxide and then planarized with CMP and HDP oxide densification at 1000°C/30min. Nitride removal and well implantation steps were then followed.

### Twin Well Formation

Diffused twin wells were formed by implanting phos. 160keV/1.5E13 for the n-well and BF<sub>2</sub> 60keV/2E13, using a 1200°C/100min well drive-in to achieve 4.0μm deep wells. Shallow retrograde wells were formed by implanting boron 300keV/1.2E13 for the p-well and phos. 500keV/2E13 for the n-well with a 1000°C/30min anneal to achieve 1.1μm deep wells. Deep retrograde wells were formed by implanting boron 500keV/1.2E13 for the p-well and phos. 800keV/2E13 for the n-well with a 1000°C/30min anneal to achieve 2.0μm deep wells. BL/CL retrograde wells had one additional implant. A blanket boron buried layer implant between 1.5 to 1.7MeV at doses from 3E13 up to 4E14 and the p-well connecting implant was achieved by increasing the deep p-well boron implant from 500keV to 800keV/3E13. This required a thicker photoresist mask of around 4μm thick to completely block the 800keV boron ion. BILLI retrograde wells had one less mask (no p-well mask). The n-wells and p-wells were both formed with the same n-well mask, using mutiple chained implants clustered

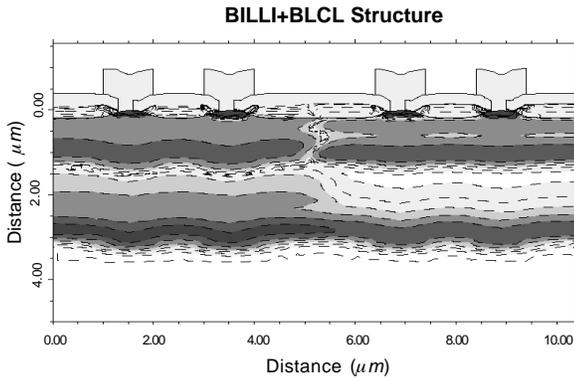


Fig 1. 2-D modified BILLI (BILLI+BL) twin well dopant profile.

together. A thinner photoresist of 2.3μm was used and along with boron energies up to 2.0MeV to form the deep p-well. A modified BILLI retrograde well (BILLI+BL) was achieved by adding a blanket boron buried layer implant at 1.7MeV (shown in Fig 1).

### Triple Well Formation

Both the diffused triple well and the hybrid (sub-MeV + diffusion) triple well were formed by 500keV phos. implant, followed by a 1200°C/3 hour drive-in anneal to form a 5.3μm deep n-well. Standard twin retrograde n and p-wells were formed on top. The MeV triple well was formed with a 2.0 to 2.2 MeV phos. implant resulting in a deep n-well at 2.7μm deep and Rp at 1.7μm. Standard retrograde twin wells were then patterned and formed on top. The BILLI triple well was formed similarly to the MeV triple well. This was done without the p-well mask implant of the twin well as described in the BILLI twin well formation above (see Fig 2).

## III. RESULTS

### LOCOS Isolation Latch-up Results

Results on vertical current gain ( $B_V$ ) for various n<sup>+</sup> to p<sup>+</sup> spacing are shown in Fig 3. Note the increase in  $B_V$  for both diffused well and retrograde well structures for <3.5μm n<sup>+</sup> to p<sup>+</sup> spacings. Lateral current gain ( $B_L$ ) results are shown in Fig 4. Note the steep rise in  $B_L$  for n<sup>+</sup> to p<sup>+</sup> spacing: <3.5μm for both the retrograde well and BL/CL cases. This was due to the

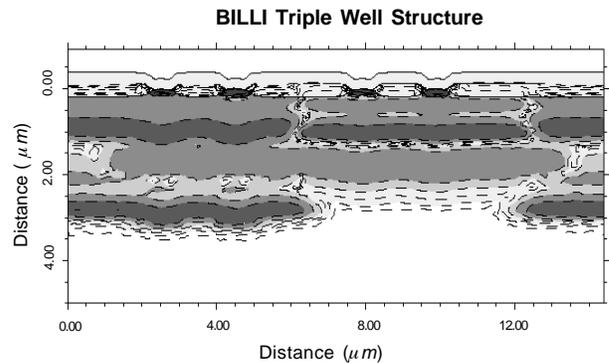


Fig 2. 2-D BILLI triple well dopant profile.

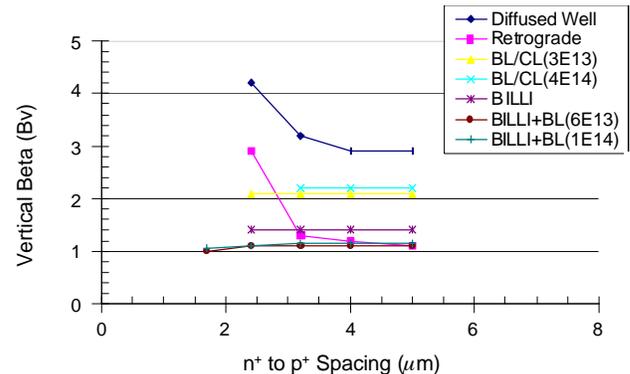


Fig 3. LOCOS vertical beta latch-up results.

electric field effect similar to epi-wafers. Results on p<sup>+</sup> trigger current are shown in Fig 5. As the n<sup>+</sup> to p<sup>+</sup> spacing drops below 4μm, note the rapid drop in p<sup>+</sup> trigger current for the BL/CL structure. However, the modified BILLI structure showed excellent p<sup>+</sup> trigger current down to 1.5μm spacing. The modified BILLI structure also showed excellent n<sup>+</sup> trigger current down to 1.5μm spacing (see Fig 6). Fig 7 shows results from holding voltage (V<sub>H</sub>). The best V<sub>H</sub> is shown for the modified BILLI structure.

### STI Isolation Latch-up Results

Results on vertical current gain (B<sub>V</sub>) for various n<sup>+</sup> to p<sup>+</sup> spacing are shown in Fig 8a. Note the increase in B<sub>V</sub> for retrograde well structures for decreasing n<sup>+</sup> to p<sup>+</sup> spacings, while the BILLI, BL/CL and modified BILLI structures all had

higher B<sub>V</sub>. This was due to the shallower n-well being compensated by the p<sup>+</sup> buried layer under the n-well. Lateral current gain (B<sub>L</sub>) results are shown in Fig 8b. Note that B<sub>L</sub> was 2.5x lower for the BILLI structure, compared to the retrograde well and both the BL/CL and modified BILLI structures were an additional 2.5x lower. Results on p<sup>+</sup> trigger current are shown in Fig 9. Note how flat the p<sup>+</sup> trigger current values are for the modified BILLI all the way down to 0.8μm spacing, though the values are higher for the BL/CL structure. The modified BILLI structure and BILLI structures both showed excellent n<sup>+</sup> trigger current down to 0.8μm spacing (see Fig 10). Also, the holding voltage (V<sub>H</sub>) results for the modified BILLI and BL/CL structures show excellent results down to 0.8μm with STI (see Fig 11).

### Triple Well

Superior NMOSFET narrow width effects in a BILLI triple well are shown in Fig 12. Also p-well to triple p-well breakdown voltages were the same between MeV triple well and BILLI triple well structures.

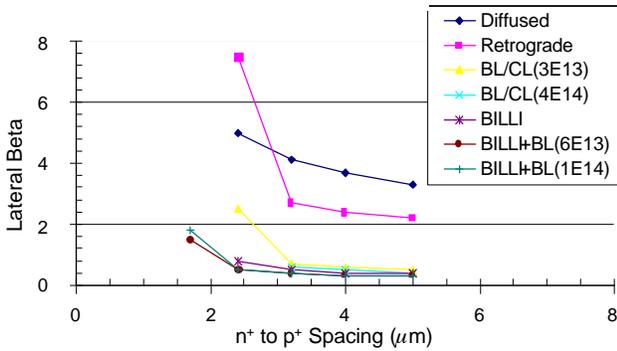


Fig 4. LOCOS lateral beta latch-up results.

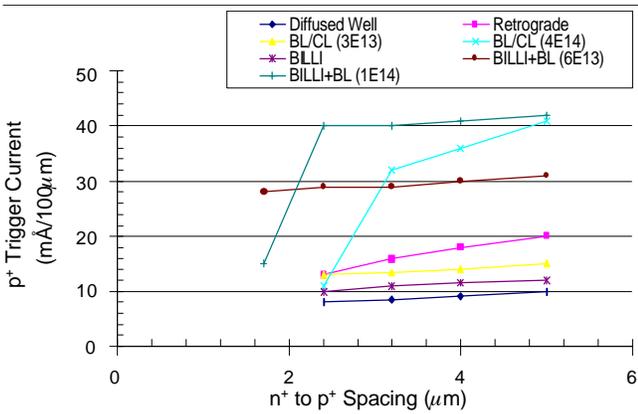


Fig 5. LOCOS p<sup>+</sup> trigger current latch-up results.

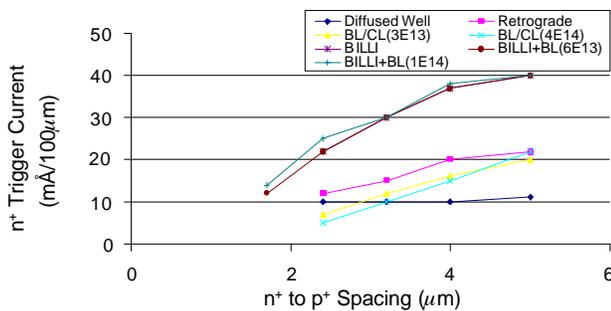


Fig 6. LOCOS n<sup>+</sup> trigger current latch-up results.

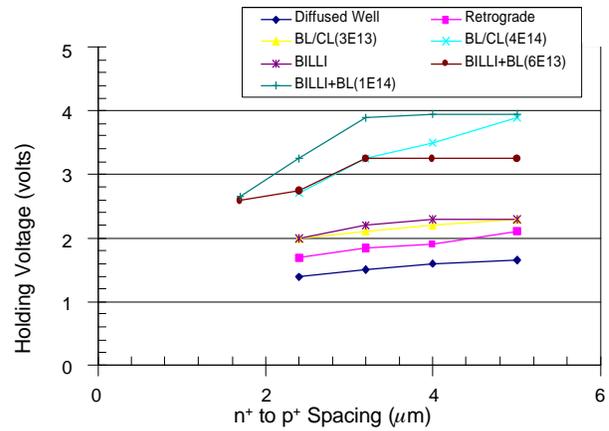
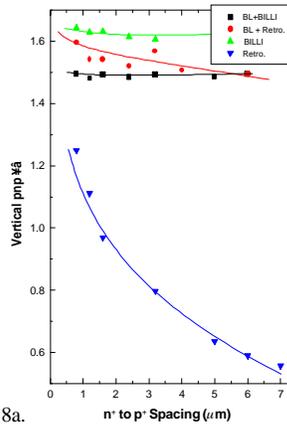
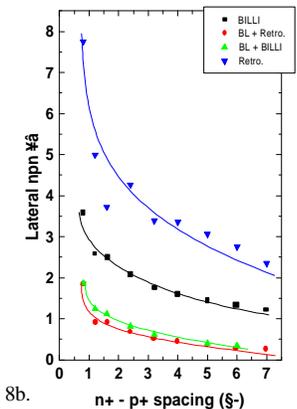


Fig 7. LOCOS holding voltage (V<sub>H</sub>) latch-up results.



8a.



8b.

Fig 8. STI latch-up results, a) vertical current gain B<sub>V</sub> and b) lateral current gain B<sub>L</sub>.

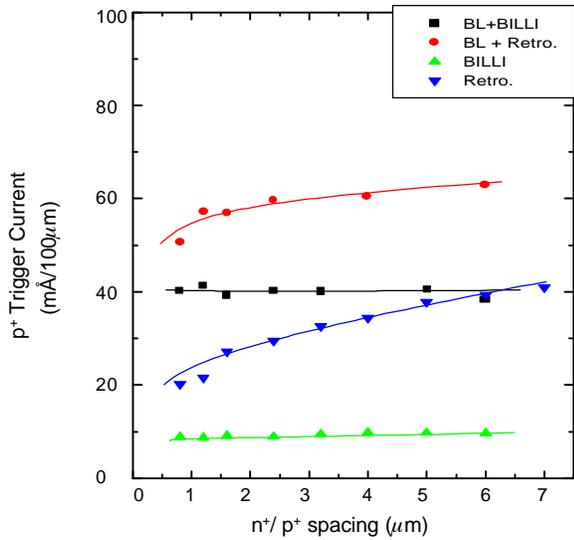


Fig 9. STI p<sup>+</sup> trigger current latch-up results.

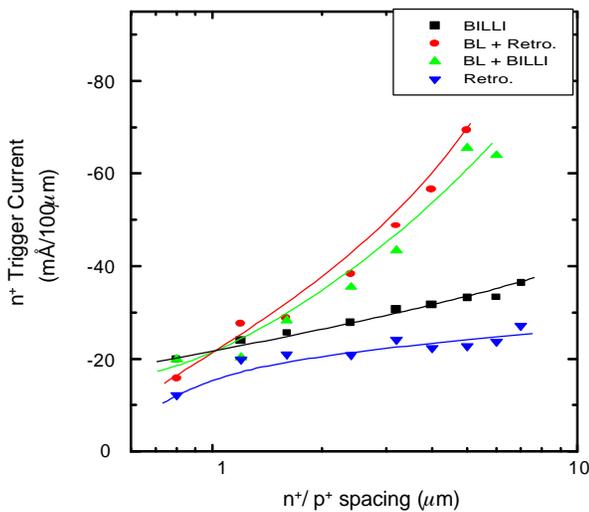


Fig 10. STI n<sup>+</sup> trigger current latch-up results.

Junction leakage data showed that n-well to substrate leakage was bad for a 1.5MeV boron blanket buried layer implant at both 3E13 and 4E14 (2E-14 and 1E-14Å/µm<sup>2</sup> respectively). With a 2MeV BILLI boron implant at 3E13 dose, the leakage was good at 4E-17Å/µm<sup>2</sup>.

#### IV. CONCLUSION

Use of the modified BILLI structure (BILLI+BL) allows the extendibility of LOCOS type isolation down to 0.2µm technology in device manufacturing, and it is possible to maintain excellent latch-up performance at tight n<sup>+</sup> to p<sup>+</sup>

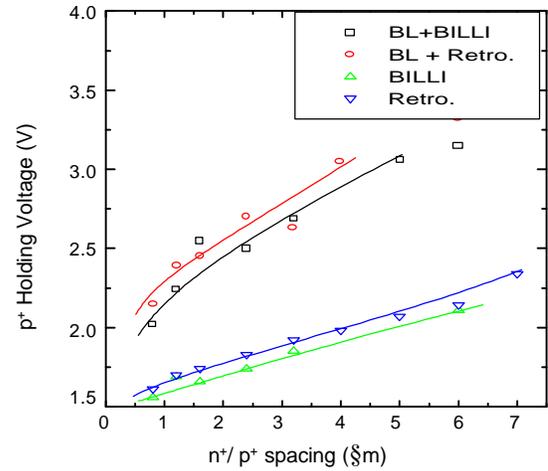


Fig 11. STI holding voltage ( $V_H$ ) latch-up results.

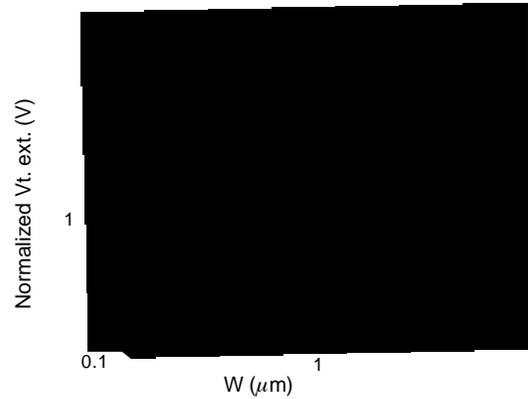


Fig 12. Triple well NMOSFET narrow width effects.

spacing. This method also provides process simplification, which results in lower cost manufacturing. With STI (shallow trench isolation) we have shown latch-up performance down to 0.8µm n<sup>+</sup> to p<sup>+</sup> spacing, which is required for 0.18µm device technology. The BILLI structure has also been applied to triple well structures resulting in excellent device characteristics.

#### REFERENCES

- [1] Satoshi Shnozski, IEDM 96 DRAM short course, Dec. 1996.
- [2] John Borland, BILLI U.S. patent #5,501,993 (March 1996), #5,814,866 (Sept. 1998) and #5,821,589 (Oct. 1998).

