Epi Replacement and up to 30% Process Simplification in a CMOS Foundry Environment Using the BILLI Structure

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Abstract- We report for the first time a reduction of up to 30% in front end processing steps and the potential elimination of epi wafers from a typical CMOS twin well process scheme. This was achieved through process integration and optimization of the BILLI technology while maintaining all standard device parametrics. We will show our process integration methodology and device parametric tuning results as a function BILLI implant energy, dose and species in forming the twin n-well and p-well structures. Consequently, the BILLI process has commenced implementation in manufacturing, allowing us to pass on significant benefits to our customers in reducing both cost and cycle time, and be very competitive in the foundry business.

I. Introduction

A typical 0.7μm high performance mixed signal CMOS process may incorporate a diffused twin well self-aligned process. To achieve this the front end requires five masking levels, six implants and numerous diffusion steps. The Genus 1520 MeV system, however, provides the capability of producing deep wells using a BILLI process without the need for an extensive drive-in step. This allows a substantial simplification in front end processing, providing great benefits to its customers. This is particularly important for emerging, novel devices, where the size of the potential market is dominated by die cost, but other device considerations do not allow 0.5/0.35μm or below geometries to be used. Another significant benefit to the customer is the reduction in fab cycle time associated with process simplification. Through a cooperative Joint Development Project (JDP) between Genus and Newport Waferfab Limited we have shown the potential elimination of epi wafers to be possible, and have reduced front end processing by 30% using the BILLI structure [1]. This will allow us to achieve the manufacturing cost targets required for many foundry customers.

II. Process Integration

A comparison of the key sections of the process in which differences occur between a typical diffused twin well versus the BILLI process is shown in Table I, and these are shown schematically in Figs 1 and 2, respectively.

Despite the obvious advantage in terms of process simplification, concerns remained that the modified heat cycle employed would result in stacking fault problems following the field oxide process, and the possibility of a reduction in Gate Oxide Integrity (GOI). Furthermore, with the additional removal of the epi substrate, latch-up characteristics would need to be reviewed.

Another advantage of BILLI is that during well formation for the standard diffused twin well process, a step height is formed between the n-well and p-well regions. This develops as a result of different oxidation rates of implanted $Si0_2$. This step is removed when the BILLI process is used.

In order to permit the BILLI process module to be integrated into the standard CMOS process, key stages of learning were required. These were:

- implant profiling
- electrical parameter matching
- functional testing

The approach employed for the investigation, and the results obtained, will de described.

III. Methodology and Results

Implant Profiling

The initial stage of integration of the BILLI process was to establish the implant profiles obtained in silicon using the high energy Genus implanter. It is clear that when using the BILLI process, there is a requirement for some implants to penetrate photoresist before entering the substrate. The stopping power and thickness of resist is, therefore, critical and needs to be closely monitored. Any deviation in photoresist thickness will result in a variation in implant depth, and hence parametric performance. In order to determine the stopping power of the photoresist, initial characterisation work was performed by carrying out implants (see Table II for details) through 400Å sacrificial oxide and 6000Å field oxide films, with and without photoresist in place. The dopant profiles were verified using SIMS analysis.

The summary of the implant peaks (Rp) are shown in Figs 3 and 4 for boron and phosphorus implants. Resist thickness uniformity was seen to be tightly enough controlled to produce

no significant effects on implant profiles. From these results, suitable implant energies could be estimated for each implant to match the characteristics of the standard process.

TABLE I.
Comparison of typical and BILLI processes.

Diffused Twin Well	BILLI Process
Initial Oxide	Miss
Initial Nitride	Miss
N-Well Photo	Miss
Nitride Etch	Miss
N-Well Implant - Phos	Miss
Resist Strip	Miss
Masking Oxide	Miss
Nitride Etch	Miss
P-Well Implant -	Miss
Well Drive-In	Miss
Oxide Removal	Miss
Pad Oxide	Pad Oxide
Pad Nitride	Pad Nitride
Active Area Photo	Active Area Photo
Nitride Etch	Nitride Etch
Field Implant Photo	Miss
Field Implant - Boron	Miss
Resist Strip	Resist Strip
Field Oxide	Field Oxide
ONO Removal	ONO Removal
Sac Oxide	Sac Oxide
Miss	N-Well Photo
Miss	P-Well Implant -
Miss	NPT Implant - Boron
Miss	VTN Implant - Boron
Miss	N-Well Implant -
Miss	PPT Implant Phos
Miss	VTP Implant - Boron
Miss	Resist Strip
VTN Photo	Miss
VTN Implant - Boron	Miss
NPT Implant - Boron	Miss
Resist Strip	Miss
VTP Photo	Miss
VTP Implant - Boron	Miss
Resist Strip	Miss
5 Masks	**2 Masks**
6 Implants	**6 Implants**
28 Process Steps	**16Process Steps**

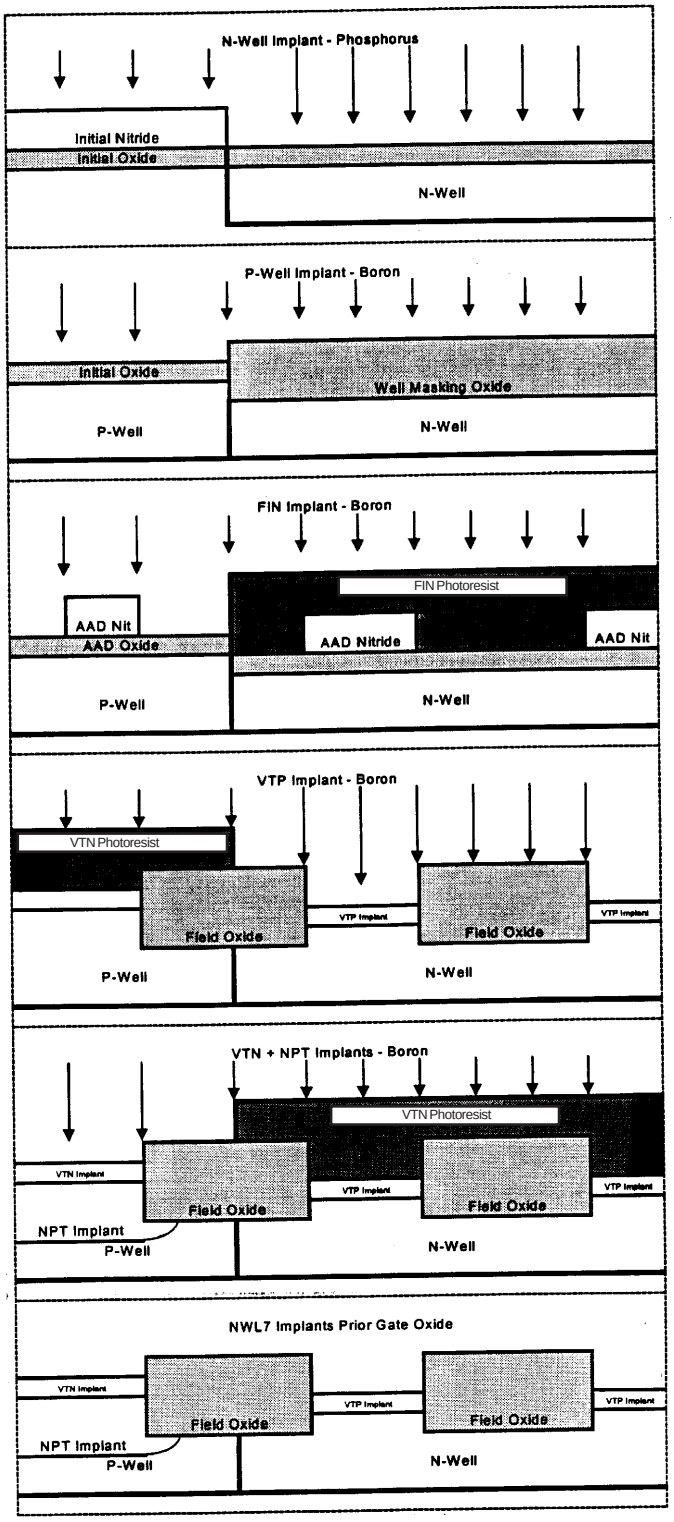

Fig 1. Schematic of diffused twin well process flow.

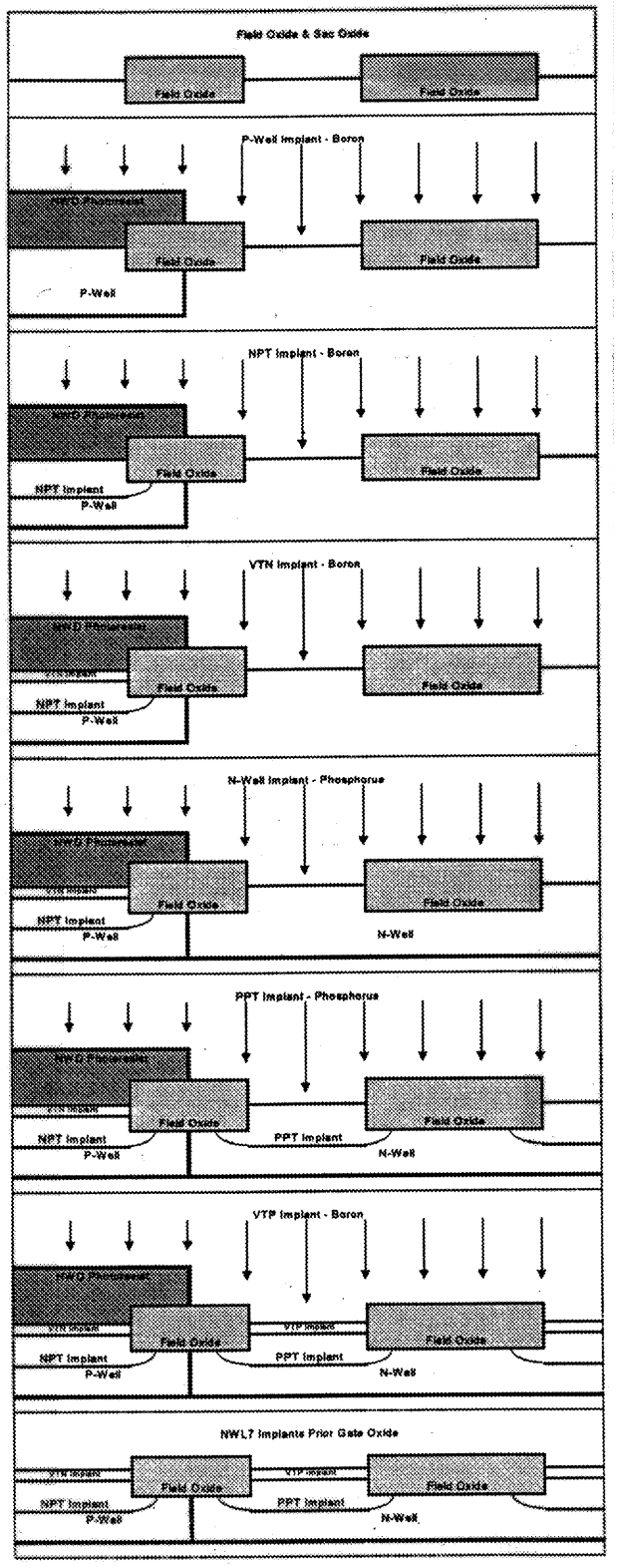

Fig 2. Schematic of BILLI process flow.

Electrical Parameter Matching

In order to match the electrical parameters of the standard process using the BILLI option, a number of implant split lots were processed using a range of doses and energies. These were identified from the results of the previous work, and aimed

TABLE II.
Details of implants for profile analysis.

Implant	400A Sac Ox	1.8µm PR 400A Sac Ox	6000A LOCOS	1.8µm PR on LOCOS
P=1MeV/2E13	X		X	
P=500keV/5E12	X		X	
B=30keV/2E12	X		X	
B=1.9MeV/3E13	X	X	X	X
B=1.4MeV/5E12	X	X	X	X
B=1.2MeV/5E12	X	X	X	X
B=1MeV/5E12	X	X	X	X
B=900keV/2E12	X	X	X	X
B=800keV/2E12	X	X *	X	X *
B=700keV/2E12	X	X	X	X

Note: Four wafers were processed in order to assess the photoresist thickness repeatability.

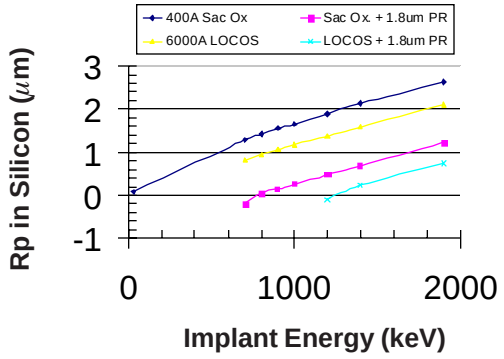

Fig 3. Boron implant profiles for BILLI processing

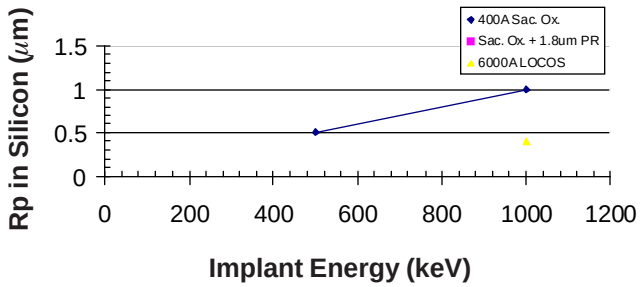

Fig 4. Phosphorus implant profiels for BILLI processing.

to determine the optimum dose and energy required for each implant.

Once these were established, wafers could be run for which all implants were more closely matched to the standard material. Several identical lots were run to assess repeatability of results. Splits were carried out on both epi and non-epi substrates. Examples of the parametrics achieved for various split combinations are given in Table III.

It can be seen from the results that the electrical parameters could be matched almost exactly to standard material with split 1, with the exception of the n-well resistance. It was felt, however, that this would be acceptable for functionality testing. It was also found that PVt could easily be adjusted by variation of this implant. Split 2 produced an almost matched Vt process. However, if this parameter was reduced too far, leakage was seen to increase significantly.

TABLE III.
Electrical parameters for standard and BILLI splits.

SPLIT	STD		SPLIT 1		SPLIT 2		SPLIT3	
Silicon	Epi	Non-epi	Epi	Non-epi	Epi	Non-epi	Epi	Non-epi
NVt	650	646	715	707	710	713	610	613
PVt	-918	-914	-918	-921	-776	-779	-508	-526
N Ids	9870	9905	9165	9190	9300	9185	9885	9750
P Ids	4660	4685	4245	4270	4680	4610	5100	5015
Nleak	0.62	0.07	0.33	0.06	0.06	0.41	323	370
Pleak	0.09	0.06	0.06	0.06	0.17	0.132	421	396
Nbd	-19	-19	-19	-19	-19	-19	-19	-19
Pbd	-17	-17	-18	-18	-18	-18	-17	-18
Nleff	0.59	0.6	0.61	0.62	0.62	0.61	0.6	0.61
Pleff	0.77	0.77	0.79	0.79	0.8	0.8	0.82	0.81
Nweff	0.74	0.74	0.76	0.74	0.75	0.75	0.78	0.77
Pweff	0.77	0.77	0.78	0.77	0.75	0.75	0.75	0.74
Rnwell	2892	2998	659	657	1610	1595	642	635

N/PVt	Threshold voltage (mV)
N/PIds	Source-drain current (μÅ)
N/Pleak	Junction leakage (nÅ)
N/Pbd	Gate breakdown (V)
N/Pleff	Effective transistor length (μm)
N/Pweff	Effective transistor width (μm)
Rnwell	N-well resistance (ohm/sq)

No significant difference was observed between parametrics from the epi and non-epi wafers. Repeatability between wafer batches was also seen to be very good.

In addition, the following were determined in respect of stacking faults, GOI and latchup characteristics:

Stacking Faults: there were no stacking fault problems detected on either epi or non-epi silicon.

GOI: the GOI of BILLI material was measured and fell within the normal distribution of material in line.

Latch-Up: the standard process produced a holding voltage of ~12.5V compared to ~9.6V to ~11.3V for BILLI material, depending on the p-well energy. This difference, however, is not believed to be of concern for the majority of applications.

Functionality Testing

Following this successful parametric matching using the BILLI process, functionality testing was performed. Results were very encouraging. In all cases, functionality was not seen to be impaired by the use of the BILLI module.

However, the reduction in n-well resistance had a significant effect for devices reliant on n-well resistors. The requirement could be satisfied, however, by including an additional mask and implant for the n-well resistor areas only. This has not been performed to date.

IV. CONCLUSION

It has been shown that the total number of front end process steps is greatly reduced using the BILLI process. The overall comparison is shown below:

Typical CMOS Process	49 process steps
BILLI Process	33 process steps 33% saving
BILLI Process (+N-Well)	37 process steps 24% saving

It is very difficult to put a definitive financial savings on the reduction of process steps due to the effects of the fab loading/process mix, but it is clear that the potential is significant. Furthermore, the Genus implants could be chained together, thus further reducing the number of process steps and improving fab cycle time.

In addition to the decrease in processing costs, an initial set-up cost saving to the customer of at least the price of two or three reticles (~$2000-3000) is guaranteed. The elimination of epi substrates as the starting material will also provide a baseline economy.

The standard Fab 1 core process now has the option to be significantly simplified using the BILLI process with a reduction of up to 12 process steps and 3 photo masks being possible. The electrical parameters of the standard Diffused Twin Well process have been replicated almost exactly with the BILLI process which provides acceptable latch-up and GOI parameters. The reduced n-well resistance value could be increased, if required, with the use of an additional n-well resistor mask. It is anticipated that these improvements will be attractive to many customers in the foundry market.

REFERENCES

[1] John Borland, BILLI U.S. patent #5,501,993 (March 1996), #5,814,866 (Sept. 1998) and #5,821,589 (Oct. 1998).