Hydrogen Denudation For Enhanced Thin Oxide Quality, Device Performance, and Potential Epitaxial Elimination

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Abstract

We report on the use of hydrogen denudation processing (annealing) that significantly improves CMOS bulk Cz wafer quality. Superior device performance, thin tunnel/gate oxide quality and Cz wafer surface properties have been measured demonstrating the potential for epitaxial elimination. This is achieved by subjecting the wafers to a short hydrogen denudation pre-process between 1050 C and 1200 C for 15 to 30 minutes. For thin oxides down to 8.2 nm up to 29% improvement was observed on two different QBD structures. Hydrogen denuding was also very effective in eliminating mode B oxide breakdown failures on bulk non-epitaxial Cz wafers. Additionally, an order of magnitude decrease in junction leakage was observed for the H_2 annealed wafers relative to the bulk non-epitaxial Cz wafers, resulting in bulk Cz wafers with surface properties similar to epi wafers without the added cost. SIMS and thermawave analysis coupled with an MeV phosphorus implant were used to characterize the effect of H_2 anneal on interstitial oxygen at the surface.

Introduction

Deep submicron CMOS technology is switching from a high temperature diffused well to a low temperature MeV technology [1-5]. For MeV processing a denudation step must be added or incorporated into the process flow [6]. An inert denuding ambient is superior to an oxidizing ambient and hydrogen has been reported to be the best [7-9]. Recently a significant breakthrough in bulk Cz wafer quality was reported by using hydrogen annealing/denudation resulting in the realization of surface properties similar to that on epi wafers without the added cost [10].

The realization of reliable thin gate oxide and thin tunnel oxide less than 10 nm thick is very difficult task for deep submicron technology and is extremely sensitive to the silicon surface condition such as residual surface impurities, Si surface termination, near crystallographic defect, and point defects. One method to characterize oxide integrity is breakdown histograms. This well established method categorizes failure modes as either mode A, mode B, or mode C. Mode C failures represent intrinsic oxide breakdown while mode A failures are related to surface foreign material such as unintentional contaminants, impurities and particles. Mode B failures on the other hand are related to silicon material crystallographic defects such as as-grown stacking faults and SiOx precipitates and process induced crystallographic defects. Having a region free of defects and interstitial oxygen (denuded zone) will result in the elimination of mode B failures and this is routinely achieved by using an epitaxial layer as a denuded zone [8]. However, until just recently comparable results could not be achieved with just bulk Cz wafers (non-epitaxial). Using an inert ambient such as hydrogen with annealing at temperatures as high as 1200 C for 1 hour, elimination of mode B failures have been reported [10]. However, in this study, we report on much shorter hydrogen annealing times and temperatures down to 1050 C and report on the denudation effectiveness from a defect prevention perspective.

Experimentation

Pre-process hydrogen denuding was achieved by annealing standard p- Cz wafers in a hydrogen ambient for 15 or 30 mins. at 1050, 1100, 1150, 1200 C in an AMC-7810 epi reactor. Following this, the wafers were either; 1) ion implanted with phosphorus at 1Mev/5e14 dose and annealed for denudation analysis or, 2) processed for oxide reliability testing and QBD structure formation.

Results

A. Oxide Reliability:

Shown in figure 1 is a Mode B, C histogram analysis of epi wafers, std CZ wafers without H_2 annealing and H_2 annealed wafers at 1150 C for 30 min. The capacitor area consisted of 2.4 mm^2 area with a gate oxide thickness of 18 nm. Each histogram represents 166 capacitors. An impressive elimination of mode B failures (BV range of 7-18 volts) was observed. This statement can be made since both the epi wafer and 1150 C histograms only produced 2 mode B failures at most, while std CZ wafers without epi produced 30 mode B failures. These results have far reaching implications for deep sub-micron CMOS processing since the epitaxial layer may be eliminated utilizing the Hydrogen annealing technique.

QBD analysis consisted of a ultra thin oxide of 8.2 nm that is used as a tunneling oxide. Figure 2 displays the bulk structure which displayed a dramatic increase in bulk QBD from 8.0 to 10.33 coul/cm^2 (29% increase) as the hydrogen annealing temperature was increased from 1050 to 1200 C. Additional QBD analysis consisted of a S/D EDGE structure (Figure 3) that consisted of a serpentine S/D structure that contained a large area of LOCOS EDGE. Once again a substantial increase in EDGE QBD was obtained with the H_2 anneal. Both structures displayed a significant 12% improvement in oxide quality over our standard high quality tunnel oxide without H_2 annealing.

B. Denudation Effectiveness:

Figure 4 shows SIMS analysis results where the oxygen pile-up at the implant R_p can be reduced by two orders of magnitude from 1.5E14/cm^2 to 1.8 E12/cm^2 by

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using the hydrogen denudation pre-processing. Results from therma-wave analysis also confirmed defect recovery. As-implanted TW# was 2576, 1050 C denudation wafer after anneal TW# was 96 and the 1150 C denudation wafer had a TW# of 37.

C. Diode Leakage Current:

A sizable reduction in leakage current in the n^+ silicon region was observed when the 1150 C H_2 annealed wafer was contrasted with the non H_2 annealed Cz wafers (figure 5). Also shown in the comparison is a curve representing the background signal obtained with the probe disconnected.

Summary/Conclusion

The impact of adding a hydrogen anneal prior the first oxidation in CMOS processing has demonstrated the elimination of mode B failures and enhanced oxide integrity. Additional improvements were obtained with improved junction leakage measurements indicating improved device performance levels. Oxide reliability and denuded zone analysis confirms that H_2 annealed Cz wafers are equivalent to epitaxial wafers without the added cost (up to $100/wafer on 8" substrates). These results have immense potential cost savings for all CMOS fabrication areas today currently using epitaxial substrates especially when applied with MeV technology.

Acknowledgments

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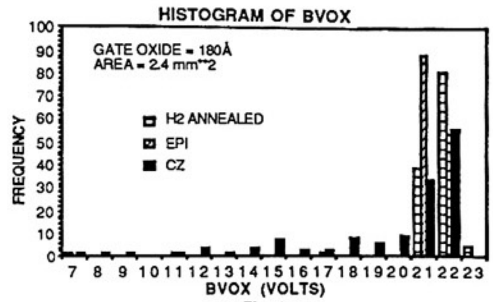

Fig. 1

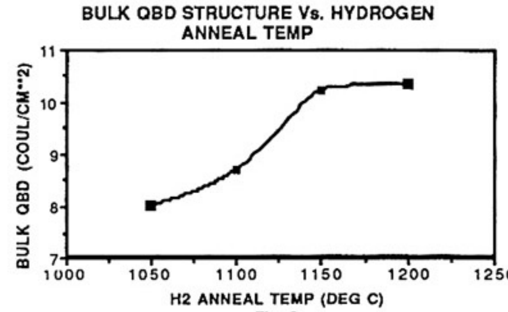

Fig. 2

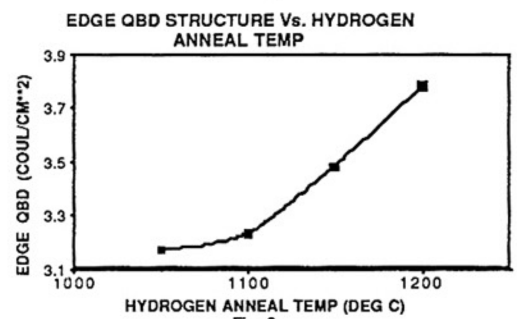

Fig. 3

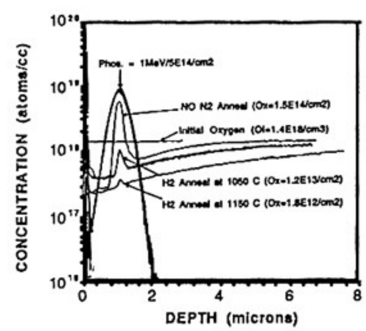

Fig. 4

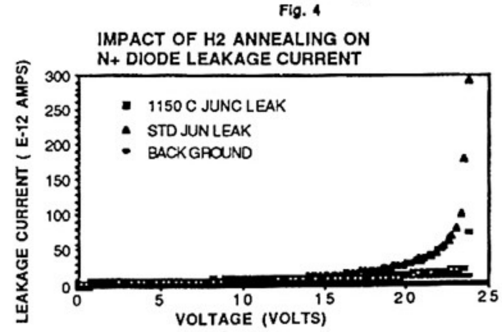

Fig. 5