ACTIVATION OF THE INTRINSIC GETTERING MECHANISM BY THE GROWTH OF OXYGEN RELATED PRECIPITATES IN CZ-GROWN SILICON WAFERS

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Abstract

Activation of the intrinsic gettering mechanism in a three-step preprocessing heat treatment was monitored by minority carrier lifetime measurements on MOS fabricated capacitors. Changes in the interstitial oxygen concentration and micro-defect generation in the bulk of the wafers were also used to monitor the degree of oxygen precipitation. For Cz-grown material, the third step of the heat treatment cycle was responsible for inducing oxygen precipitation growth and it was this step which activated the intrinsic gettering mechanism. An improvement in lifetime by over three orders of magnitude was achieved. Applications of gettering to CMOS Bulk and Epi technologies are also presented.

Introduction

One of the key inhibitors to processing very high speed devices are crystallographic imperfections (defects) located in the active regions of VLSI devices. These defects exist in a large variety of forms ranging from impurity atoms to macro-precipitates and dislocations. If these defects are located in an inactive region of the wafer, they act as gettering sites by trapping the unwanted impurities and defects away from the device active region, thereby improving device performance and yield (1). A three-step heat treatment is presented that achieves intrinsic gettering with bulk SiOx precipitation and a well defined denuded zone.

Gettering in silicon is the process of cleaning up the near surface device active region of impurities and trapping them in the bulk of the wafer (2). Micro-defects are introduced into the silicon lattice as grown-in defects during single crystal Czochralski (Cz) growth or during the numerous device processing steps (3). Creating a defect-free surface (denuded zone) where the device is formed and bulk gettering sites, requires several thermal processes. In intrinsic gettering, the intrinsic material properties of silicon are used to activate the getter mechanism that traps the unwanted impurities in the wafer (4). This is accomplished by using the supersaturated interstitial oxygen (Oi) located in the silicon wafer and inducing

SiOx micro-precipitation. These precipitates generate lattice disorder and defects which act as traps (getter sites) for the impurities.

The mechanism and driving force for gettering is not fully understood. However, the activation of the getter sites has been detected and will be presented herein.

Experimentation

Boron-doped, 5-7 Ω-cm, P(100), 100mm diameter Cz-grown wafers approximately 525 microns thick, front-side polished were used. Wafers from the same Siltec ingot were sawn and laser marked in numerical order to maintain ingot and wafer position identity, allowing experimental comparison of adjacent and therefore nearly equivalent wafers. A Siltec 108 single phase AC furnace with a 10.8 kilogram charge was used to grow three ingots. A flat shoulder growth process was used with a 16 rpms counter clockwise seed rotation and an 8 rpms clockwise crucible rotation. The pull speed was set at 3 inches per hour and three ingots 24 inches long were grown. All the wafers were from the region located between four and eight inches from the seed end. After slicing and laser coding, the wafers went through a resistivity stabilization anneal at 650°C for 30 minutes. Interstitial oxygen (Oi) concentrations in each wafer were measured on an FTIR (Fourier Transform Infrared) spectrometer at four locations: 1) center of the wafer; 2) 25mm; 3) 37.5mm; and 4) 44mm. Each ingot yielded a specific oxygen range. One ingot yielded wafers with high initial Oi in the range of 20 PPMA (ASTM'81), another was in the medium Oi range of 18 PPMA and the third ingot had low Oi of 16 PPMA. The carbon levels in the wafers were below the 0.2 PPMA detectability limit.

A three-step (high, low, medium temperature) thermal cycle was implemented to achieve bulk intrinsic gettering with a well defined denuded zone based on the principles of the low-high and high-low two-step gettering cycles (5). The three-step cycle was composed of: 1) denudation; 2) SiOx precipitate nucleation; and 3) SiOx precipitate growth. The denudation step was a 1150°C anneal for 4 hours in an argon plus oxygen ambient to induce oxygen out-diffusion and denuded zone formation. A 700°C anneal for 16 hours in a nitrogen ambient formed nucleation sites for SiOx precipitates and the 950°C anneal for 4 hours in a nitrogen ambient induced SiOx precipitate growth (see figure 1).

Results

Activation of the SiOx Gettering Mechanism

The three-step (high-low-medium temperature) intrinsic gettering thermal cycle achieved denudation at 1150°C with a denuded zone ~25um, nucleation of SiOx precipitate sites at 700°C and SiOx precipitate

growth at 950°C. The activation of the SiOx gettering mechanism was observed after the 950°C third heat treatment anneal which induced SiOx precipitate growth in the bulk of the silicon wafer. The extent of oxygen precipitation after each heat treatment was monitored by FTIR measurements of Oi and by Wright preferential defect etching of the (100) surface plane and (110) cross-sectional plane. Minority carrier lifetime measurements by the MOS C-t τ technique was used to monitor the getter effectiveness across the diameter of the wafers.

The impact of each heat treatment on the initial Oi content in the bulk of the wafer and changes in Oi (ΔOi) due to SiOx precipitation and/or oxygen out-diffusion were monitored by measuring the 1107 cm^{-1} absorption peak on a Nicolet MX-1 series FTIR instrument at room temperature (6). An SiO_2 characteristic peak at 1230 cm^{-1} was also monitored to determine the predominant SiOx complex precipitated in the silicon wafer (7). Figure 2 shows the change in Oi for each of the three oxygen group wafers as a function of each heat treatment. In all cases, the largest ΔOi occurred after the 4 hour anneal at 950°C. A ΔOi as much as 9 PPM was detected.

Wright etchant defect delineated (110) cross-sectional planes are shown in figures 3, 4, and 5 after each of the heat treatments in the three-step cycle. The denuded zone and micro-defects in the wafer could be delineated only after the 950°C third-step anneal. These delineated micro-defects are related to SiOx precipitates present in the bulk of the wafer (8,9).

The electrical parameters of silicon devices are affected by crystalline lattice defects in the silicon wafer, which can degrade the device (10). Typical electrical measurements, such as resistivity or mobility measurements, are not very sensitive to crystalline perfection (11). Minority carrier lifetime (τ) on the other hand is extremely sensitive to crystallographic imperfections in the silicon crystal lattice since it is a measure of either the generation lifetime or recombination lifetime of excess minority carriers (12,13,14). Crystallographic imperfections act as sites for the recombination of excess minority carriers and τ changes with each thermal anneal during device fabrication.

An MDC capacitance-time (C-t) system was used for τ measurements on wafers with fabricated MOS capacitors to monitor the degradation or improvement in surface generation τ as a function of each anneal in the three-step I.G. heat treatment (15). Nine wafers from each of the three different initial Oi ranges were subjected to the following heat treatments. The wafers from each of the three Oi groups all received a denudation heat treatment at 1150°C for 4 hours and the first three of the nine adjacent wafers from each group were removed at the end of this step while the remaining six adjacent wafers continued along the process and received the second anneal for nucleation of SiOx sites at 700°C for 16 hours. At the end of this process, the next three adjacent wafers were removed and the final remaining three wafers were

subjected to the SiOx precipitate growth step at 950°C for 4 hours. After the three-step anneal, all of the 27 wafers had 0.1 micron of an Al-Si alloy sputter deposited on top of the 700Å oxide in a dot matrix where the dot size was 2mm in diameter and 15 dots were aligned across the wafer diameter perpendicular to the major flat. The metal dots were alloyed at 400°C for 30 minutes. A consistency in radial τ profiles from adjacent wafers with identical thermal history were observed and is shown in figure 6. Therefore, to get qualitative results, it is necessary to use adjacent wafers with identical thermal history to minimize and control any intrinsic material property variation that may lead to extraneous results.

The impact of each heat treatment on the wafer lifetime is summarized below for each of the three initial Oi groups.

High Oi Wafers: A slight degradation in τ was observed in going from the denudation process to the nucleation process, but an increase (improvement) by three orders of magnitude in τ occurred after the precipitate growth process. This signifies the activation of the gettering mechanism by SiOx precipitation and growth which was induced by the third heat treatment.

Medium Oi Wafers: The same general trend in τ as mentioned above for high Oi also occurred in medium Oi wafers. No direct comparison between the three different Oi groups could qualitatively be made since they came from different ingots which may have differences in ingot growth and cooling conditions as well as wafer crystallographic imperfections.

Low Oi Wafers: Some evidence of I.G. was also observed in low Oi wafers after the third heat treatment, but the effectiveness of I.G. was minimal (see figure 7).

In summary, the results from C-t τ measurements clearly showed the activation of the intrinsic gettering mechanism only after the third heat treatment where SiOx precipitate growth occurred (see figure 8). The critical Oi level for I.G. was ~16 PPM for these wafers. Comparative analysis between radial τ variations, radial Oi variations and cross-sectional radial bulk microdefect distributions were performed. Regions of low τ after the third heat treatment corresponded to regions of low bulk precipitates and high Oi or minimal ΔOi, while regions of high τ were identified to areas of high density bulk precipitates and low Oi content. Experiments on Getter Enhanced Epitaxy have also been conducted incorporating I.G. techniques. Figure 9 shows a high τ epilayer grown on a gettered parent substrate. High quality P^- epilayer on P^+ substrates as well as N^+ epilayer on P^- substrates have been grown for advance CMOS and Bipolar technologies.

Oxygen Precipitation and Growth Gettering Mechanism

Oxygen precipitation occurs by heterogeneous nucleation at impurity particles and crystallographic imperfections in the silicon wafer.

This has been observed over the temperature ranges from 450°C to 1200°C (16). The driving force for SiOx precipitation is presented based on thermodynamic equilibrium. A system will tend to reach its lowest free energy (G) state for a given composition, temperature and other imposed conditions. Oxygen in silicon has a given solid solubility level for a specific temperature. At 950°C this solubility level was observed to be ~4.6 PPM (16). Oxygen precipitation at 950°C will occur until equilibrium is reached, then it no longer occurs, as observed in the medium and high Oi wafers after a 12 hour anneal at 950°C. SiOx precipitate formation requires a lowering of the free energy of the system, in other words, a negative ΔG. If ΔG is positive, then the opposite reaction occurs, SiOx dissolution (17). The free energy change (ΔG_r) in the system is given by:

$$\Delta G_r = 4\pi r^2 \gamma + \frac{4}{3}\pi r^3 (\Delta G_V + \Delta G_E)$$

where γ is the interface energy, ΔG_V is the free energy change per unit volume of the phase transition and ΔG_E is the strain energy per unit volume. In the expression above, $\Delta G_E = bE^2$, where E is the strain and b is a constant which depends on the shape of the nucleus.

Point defects like V_{Si} sites and carbon substitutional sites act as excellent nucleation sites because of the relaxation and inward strain field located around their site. The morphology of these SiOx nuclei and precipitates are parallel platelets, this allows precipitation to occur with minimum increase in strain energy (18). Spherical particles produce large values of strain with three-dimensional volumetric expansion (19,20,21).

These SiOx precipitates give rise to dislocation loops and extrinsic stacking faults which are the gettering vehicles. At the periphery of the stacking fault is a void which is essentially a loop of edge dislocations that traps heavy metals and other impurities in the material (negative center of dialatation). They are by products of SiOx precipitation and excellent getter sites.

Conclusion

The activation of the intrinsic gettering mechanism by the growth of oxygen related precipitates in Cz-grown wafers were detected by MOS C-t minority carrier lifetime measurements, FTIR ΔOi measurements and Wright etch defect delineation of the (110) cross-sectional plane. This gettering technique has improved the surface crystalline quality of silicon wafers used in Bulk CMOS technology and parent substrate wafers used in epitaxial growth. High quality P^- on P^+ and N^+ on P^- epitaxial layers for advance CMOS and Bipolar technologies have also been grown.

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References

1. L. Jastrzebski, IEEE Trans. Electron Devices ED-29, 475 (1982).
2. R.A. Craven and H.W. Korb, Solid State Technology 24 (7), 55 (July 1981).
3. F. Shimura and H. Tsuya, J. Electrochem. Soc. 129, 2089 (1982).
4. H. Tsuya, F. Shimura, K. Ogawa and T. Kawamura, J. Electrochem. Soc. 129, 374 (1982).
5. N. Inoue, K. Wada and J. Osaka, Semiconductor Silicon 1981, p. 282.
6. D.G. Mead, Solid State Technology 24 (11), 71 (1981).
7. S.M. Hu, Appl. Phys. Lett. 36, 561 (1980).
8. M.W. Jenkins, J. Electrochem. Soc. 124, 757 (1977).
9. M. Futagami, J. Appl. Phys. 52, 5575 (1981).
10. H. Otsuka, K. Watanobe, H. Nishimura, H. Iwai and H. Nihin, IEEE Electron Device Letters EDL-3, 182 (1983).
11. T.S. Glowinke and J.B. Wagner, J. Phys. Chem. Solids 138, 963 (1977).
12. Y. Mada, Japan J. Appl. Phys. 18, 2171 (1979).
13. F. Heiman, IEEE Trans. Electron Dev. ED-13, 781 (1967).
14. J.L. Deines, J.W. Philbrick and M.R. Poponiak, Appl. Phys. Lett. 34, 746 (1979).
15. B.J. Gordon, Solid State Technology 21, (7), 43 (July 1978).
16. J.O. Borland, these Proceedings.
17. W.D. Kingery, H.K. Bowen and D.R. Uhlmanry, Introduction to Ceramics, Secton Edition, 1976, p. 328.
18. D.R. Gaskell, Introduction to Metallurgical Thermodynamics, 1973, McGraw-Hill Book Company, p. 86.
19. F. Shimura, Y. Ohnishi and H. Tsuya, J. Appl. Phys. 51, 269 (1980).
20. S. Kishino, Y. Matsushita, M. Kanamori and T. Iizuka, Jpn. J. Appl. Phys. 21, 1 (1982).
21. S.M. Hu, J. Appl. Phys. 51, 5945 (1980).

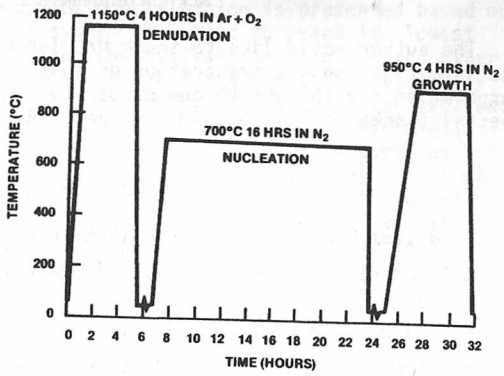


Figure 1. 3-step intrinsic gettering cycle.

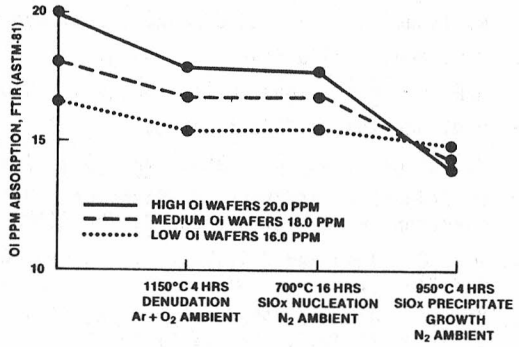


Figure 2. Change in Oi during annealing.

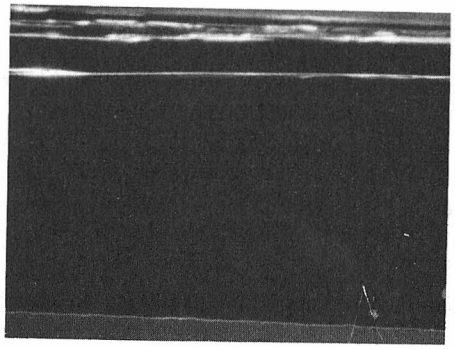


Figure 3. (110) cross-section after denudation anneal (100x).

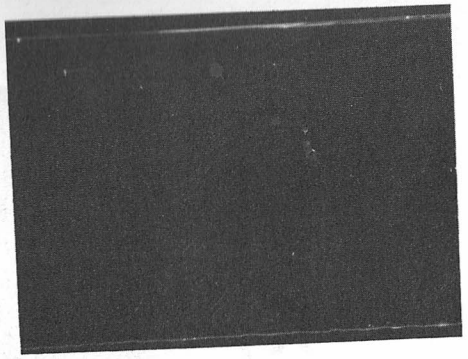


Figure 4. (110) cross-section after denudation + nucleation anneals (100x).

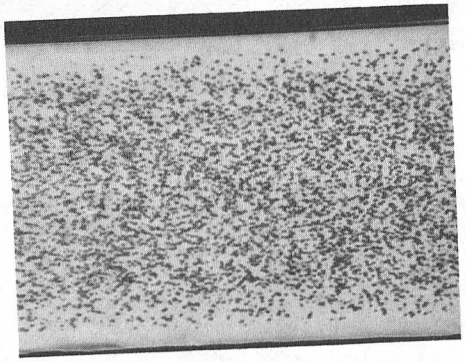


Figure 5. (110) cross-section after denudation + nucleation + precipitation, 3-step anneal (100x).

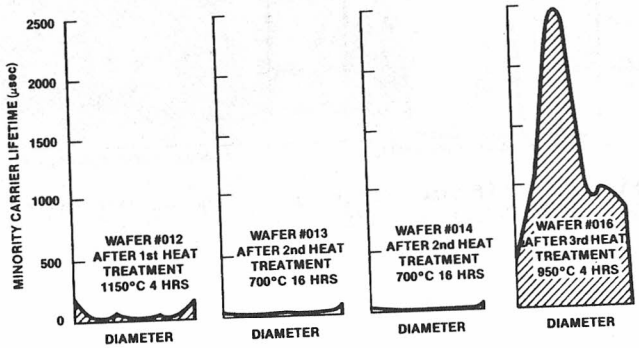


Figure 6. MOS C-t lifetime comparison of adjacent high Oi wafers.

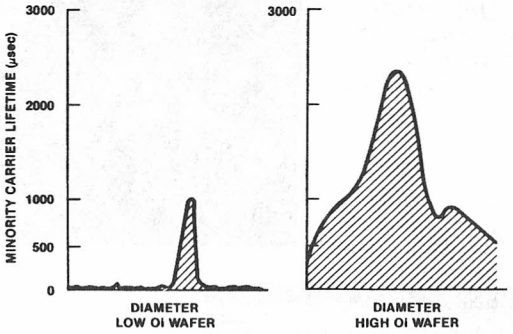


Figure 7. Lifetime comparison of low Oi and high Oi wafers after the 3-step cycle.

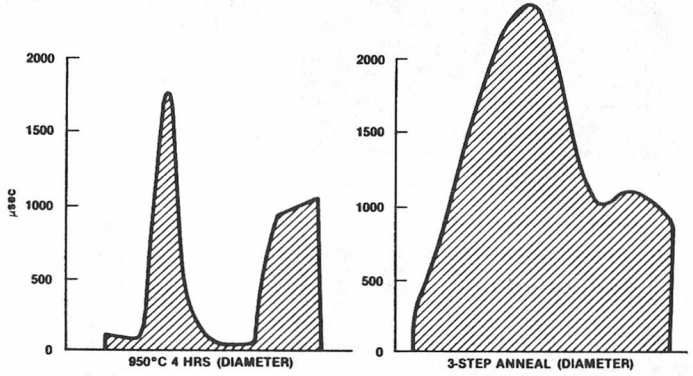
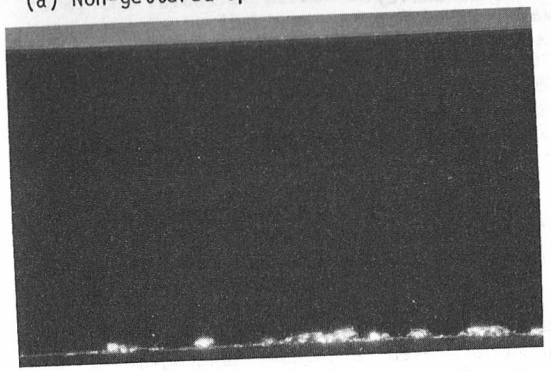
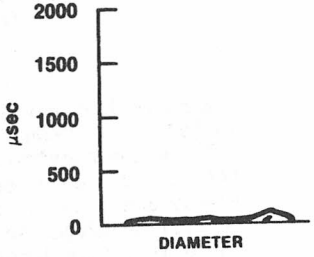


Figure 8. Lifetime comparison of high Oi wafersafter 1-step and 3-step anneals.

(a) Non-gettered epi:

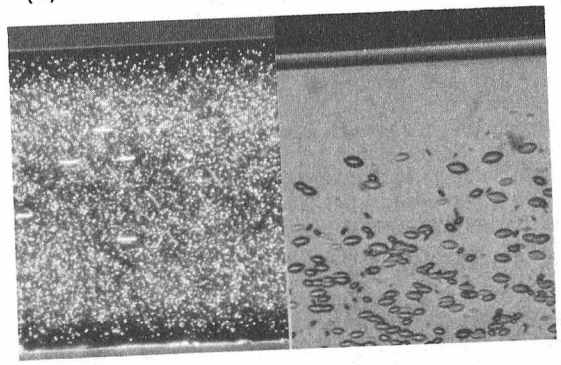


(a-1) (110) crossection (100x).



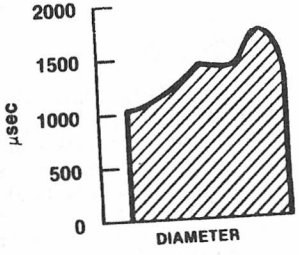
(a-2) Lifetime profile.

(b) Gettered enhanced epi:



(b-1) (110) cross-section (100x).

(b-2) (110) cross-section (400x).



(b-3) Lifetime profile.

Figure 9. Gettered vs. non-gettered P(100) 5-7 Ω·cm epilayer on P^+(100) 0.01 Ω·cm substrate.