Activation of the intrinsic gettering mechanism by the growth of oxygen related precipitates in Cz-grown silicon wafers

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Abstract

Activation of the intrinsic gettering mechanism in a three-step pre-processing heat treatment was monitored by minority carrier lifetime measurements on MOS fabricated capacitors. Changes in the interstitial oxygen concentration and micro-defect generation in the bulk of the wafers were also used to monitor the degree of oxygen precipitation. For Cz-grown material, the third step of the heat treatment cycle was responsible for inducing oxygen precipitation growth and it was this step which activated the intrinsic gettering mechanism. An improvement in lifetime by over three orders of magnitude was achieved. Applications of gettering to CMOS Bulk and Epi technologies are also presented.

Introduction

One of the key inhibitors to processing very high speed devices are crystallographic imperfections (defects) located in the active regions of VLSI devices. These defects exist in a large variety of forms ranging from impurity atoms to macro-precipitates and dislocations. If these defects are located in an inactive region of the wafer, they act as gettering sites by trapping the unwanted impurities and defects away from the device active region, thereby improving device performance and yield. A three-step heat treatment is presented that achieves intrinsic gettering with bulk SiOx precipitation and a well defined denuded zone.

Getting in silicon is the process of cleaning up the near surface device active region of impurities and trapping them in the bulk of the wafer. Micro-defects are introduced into the silicon lattice as grown-in defects during single crystal Czochralski (Cz) growth or during the numerous device processing steps. Creating a defect-free surface (denuded zone) where the device is formed and bulk gettering sites, requires several thermal processes. In intrinsic gettering, the intrinsic material properties of silicon are used to activate the getter mechanism that traps the unwanted impurities in the wafer. This is accomplished by using the supersaturated interstitial oxygen (O1) located in the silicon wafer and inducing

Results

Activation of the SiOx Gettering Mechanism

The three-step (high-low-medium temperature) intrinsic gettering thermal cycle achieved denudation at 1150°C with a denuded zone ~25um, nucleation of SiOx precipitate sites at 700°C and SiOx precipitation at 950°C.
growth at 950°C. The activation of the SiOx gettering mechanism was observed after the 950°C third heat treatment anneal which induced SiOx oxygen precipitation in the bulk of the silicon wafer. The extent of the precipitation was monitored by FTIR (infrared) absorption peaks on a Nicolet MX-1 series FTIR instrument at room temperature. An SiOx characteristic peak at 1230 cm\(^{-1}\) was also monitored to determine the predominant SiOx complex precipitated in the silicon wafer (7). Figure 2 shows the change in Oi for each of the three adjacent wafer groups as a function of each heat treatment. A significant amount of Oi as much as 9 ppm was detected.

Wright etchant defect delineated (110) cross-sectional planes are shown in figures 3, 4, and 5 after each of the heat treatments. The denuded zone and micro-defects in the wafer plane are shown in figure 6. Therefore, to get qualitative results, it is necessary to use adjacent wafers with identical thermal history to minimize and control any intrinsic material property variation that may lead to extraneous results.

The impact of each heat treatment on the initial Oi content in the bulk of the wafer and changes in Oi (\(\Delta\)Oi) due to SiOx precipitation at 950°C are summarized below for each of the three initial Oi groups.

High Oi Wafers: A slight degradation in \(C\) was observed in going from the denudation process to the nucleation process, but an increase (improvement) by three orders of magnitude in \(R\) occurred after the activation of the gettering mechanism by SiOx precipitation and growth which was induced by the third heat treatment.

Medium Oi Wafers: The same general trend in \(C\) as mentioned above for high Oi also occurred in medium Oi wafers. No direct comparison between the three different Oi groups could qualitatively be made since they came from different ingots which may have differences in ingot growth and cooling conditions as well as wafer crystallographic imperfections.

Low Oi Wafers: Some evidence of I.G. was also observed in low Oi wafers after the third heat treatment, but the effectiveness of I.G. was minimal (see figure 7).

In summary, the results from C-t measurements clearly showed the activation of the intrinsic gettering mechanism only after the third heat treatment where SiOx precipitate growth occurred (see figure 8). The critical Oi level for I.G. was \(\sim 16\) ppm for these wafers. Comparative analysis between radial \(C\) variations, radial Oi variations and cross-sectional radial bulk microdefect distributions were performed. Regions of low \(C\) after the third heat treatment corresponded to regions of low bulk precipitates and high Oi or minimal \(\Delta\)Oi, while regions of high \(C\) were identified to areas of high density bulk precipitates and low Oi content. Experiments on Getter Enhanced Epitaxy have also been conducted incorporating I.G. techniques. Figure 9 shows a high \(C\) epilayer grown on a gettered parent substrate. High quality \(P^+\) epilayer on \(P^+\) substrates as well as \(N^+\) epilayer on \(P^+\) substrates have been grown for advanced CMOS and Bipolar technologies.

Oxygen Precipitation and Growth Gettering Mechanism

Oxygen precipitation occurs by heterogeneous nucleation at impurity particles and crystallographic imperfections in the silicon wafer.
This has been observed over the temperature ranges from 450°C to 1200°C (16). The driving force for SiOx precipitation is presented based on thermodynamic equilibrium. A system will tend to reach its lowest free energy (G) state for a given composition, temperature and other imposed conditions. Oxygen in silicon has a given solid solubility level for a specific temperature. At 950°C this solubility level was observed to be ~4.6 PPM (16). Oxygen precipitation at 950°C will occur until equilibrium is reached, then it no longer occurs, as observed in the medium and high Oi wafers after a 12 hour anneal at 950°C. SiOx precipitate formation requires a lowering of the free energy of the system, in other words, a negative ΔG. If ΔG is positive, then the opposite reaction occurs, SiOx dissolution (17). The free energy change (ΔGf) in the system is given by:

\[ ΔG_f = 4\pi r^2 \gamma + \frac{4}{3} \pi r^3 (ΔG_v + ΔG_E) \]

where γ is the interface energy, ΔGv is the free energy change per unit volume of the phase transition and ΔGE is the strain energy per unit volume. In the expression above, ΔGf = bef, where e is the strain and b is a constant which depends on the shape of the nucleus.

Point defects like VSi sites and carbon substitutional sites act as excellent nucleation sites because of the relaxation and inward strain field located around their site. The morphology of these SiOx nuclei and precipitates are parallel platelets, this allows precipitation to occur with minimum increase in strain energy (18). Spherical particles produce large values of strain with three-dimensional volumetric expansion (19,20,21).

These SiOx precipitates give rise to dislocation loops and extrinsic stacking faults which are the gettering vehicles. At the periphery of the stacking fault is a void which is essentially a loop of edge dislocations that traps heavy metals and other impurities in the material (negative center of dilatation). They are by products of SiOx precipitation and excellent getter sites.

Conclusion

The activation of the intrinsic gettering mechanism by the growth of oxygen related precipitates in Cz-grown wafers were detected by MOS C-t minority carrier lifetime measurements, FTIR O1 measurements and Wright etch defect delineation of the (110) cross-sectional plane. This gettering technique has improved the surface crystalline quality of silicon wafers used in Bulk CMOS technology and parent substrate wafers used in epitaxial growth. High quality P⁺ on P and N⁺ on P- epitaxial layers for advance CMOS and Bipolar technologies have also been grown.

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References

16. J.O. Borland, these Proceedings.
Figure 1. 3-step intrinsic gettering cycle.

Figure 2. Change in O1 during annealing.

Figure 3. (110) cross-section after denudation anneal (100x).

Figure 4. (110) cross-section after denudation + nucleation anneals (100x).

Figure 5. (110) cross-section after denudation + nucleation + precipitation, 3-step anneal (100x).

Figure 6. MOS C-t lifetime comparison of adjacent high O1 wafers.
Figure 7. Lifetime comparison of low Oi and high Oi wafers after the 3-step cycle.

Figure 8. Lifetime comparison of high Oi wafers after 1-step and 3-step anneals.

Figure 9. Gettered vs. non-gettered P(100) 5-7 Ω-cm epilayer on P(100) 0.01 Ω-cm substrate.