Photovoltaics

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Webcast

Advances in Photovoltaics Manufacturing Technology

was held June 25, 2009 1PM EST
Moderator: Pete Singer Editor-in-Chief *Photolvoltaics World Magazine*

Silicon shortages are a thing of the past and crystalline-silicon (c-Si) PV cell and module manufacturers are boosting cell efficiency rates and advancing cell and manufacturing technologies. Thin film PV approaches are increasingly competitive, however, also with notable advances in efficiency.

Paula Mints
Principle Analyst PV
Services Program
Navigant Consulting

James Gee
Founder, Chief Scientist
Advent Solar

This Webcast explored these recent advances through presentations from some of the industry's most innovative companies. The presenters shared their insights and discussed the challenges ahead in photovoltaic solar cell design and process development. The discussion segment handled the issues of the day. Attendees were able to apply what they learned to maintain their company's competitive edge.

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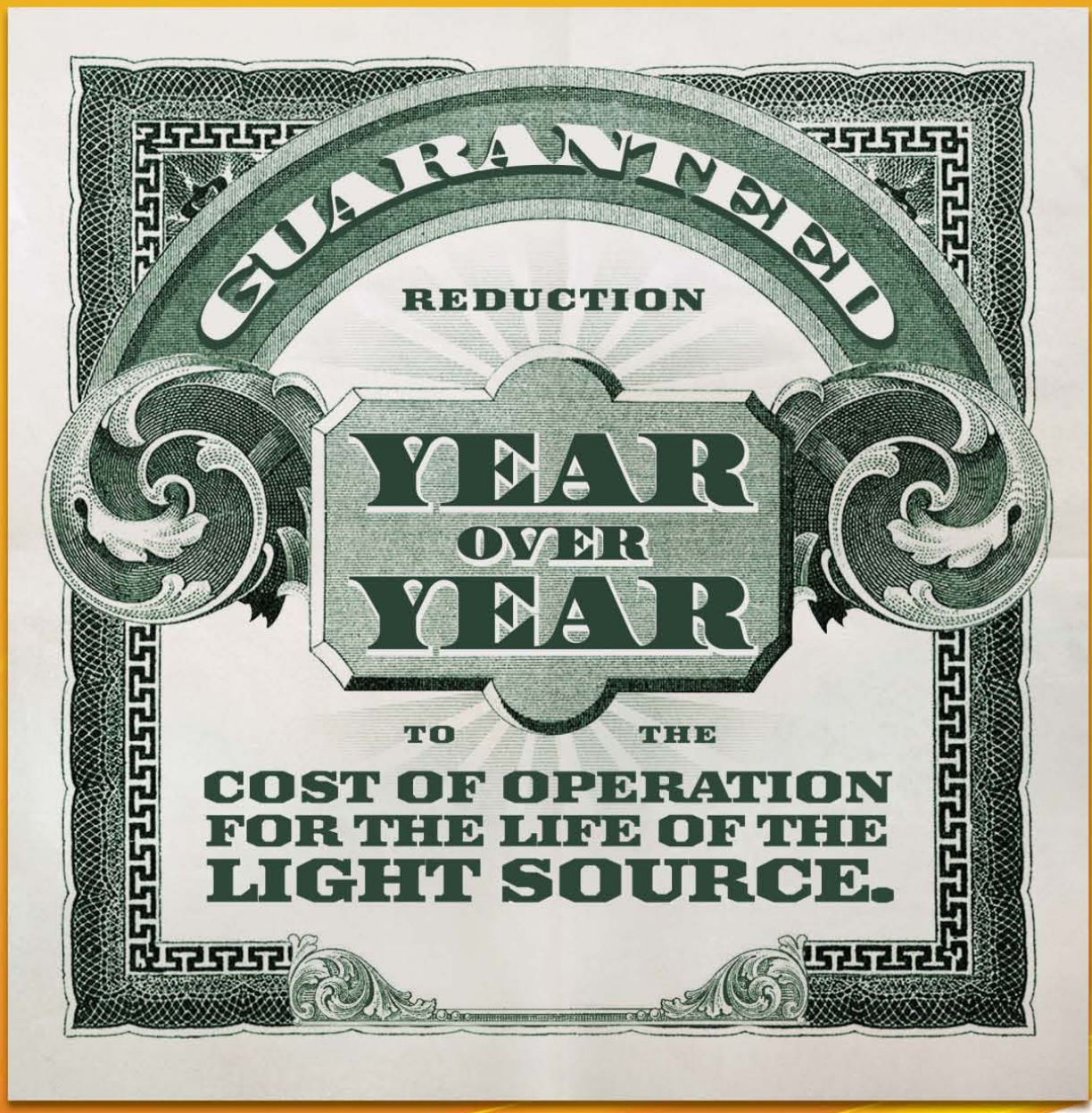

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Electrical deposition cell used for electroplating copper.
Photo courtesy of ATMI Inc. Photography by Eddie Shvartzman.

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Collaboration, manufacturing innovation vital for next-generation foundries

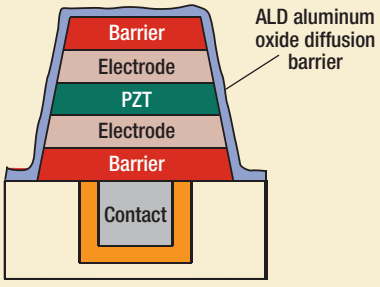
Manufacturability of advanced technology is determined by the design and the manufacturing process, but controlling these factors requires close customer collaboration, new manufacturing methods, and possibly new product design architectures. Samsung engineers discuss advancements in manufacturing using the company's S1 fab, a state-of-the-art 300mm foundry line, as an example in the areas of patterning and closed loop variation control systems.

Analyst: Buckle up for double-digit growth again

SST's Pete Singer reported from the ConFab in Las Vegas, where optimism echoed that although 2009 will be a tough year for the semiconductor industry, historic trends suggest an imminent return to double-digit growth, at least for 2010 and 2011.

ALD enables thin films for next-generation flash and NVM

ALD of high-*k* dielectrics and novel metal layers will be prevalent in producing next-generation NVMs, explain ASMI and Numonyx, because it has been shown to address many of the issues related to speed, endurance, and reliability of these devices.



Luc Van den hove helms IMEC, discusses strategy

Amid preparations for IMEC's 25th anniversary celebration, *SST*'s Debra Vogler spoke with Luc Van den hove, now president/CEO of the European R&D consortium, who discussed the research center's strategy and the keys to its success over the years.

EHS considerations in PV manufacturing equipment installations

A business risk management approach to PV equipment installation that incorporates environmental, health, and safety (EHS) considerations from the planning process through start-up can help reduce costs, minimize liability, and minimize timeframes, say Brent Wilson/EORM and Varun Gopalakrishna/Avani Design.

Reduction of PFC emissions from heat transfer fluids

This technical brief describes the use of commercially available alternative heat transfer fluids as the basis to reduce greenhouse gas emissions from microelectronic manufacturing facilities that use perfluorocarbons (PFCs) and perfluoropolyethers (PFPEs) by 58% to over 99%.

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EDITORIAL

Heard at The ConFab

For the past five years, PennWell has sponsored an event called The ConFab, which is a conference focused on semiconductor manufacturing issues, combined with a variety of focused "networking" opportunities for sponsors and delegates. It's held just outside Las Vegas at the serene and beautiful Loews Lake Las Vegas (there are shuttles to "the strip" but most attendees prefer to stay and relax).

Planning for this year's conference (held June 15-17) started in earnest last year in the late fall, with event director Jay Novack leading weekly conference calls with me and our topnotch advisory board: David Bennet (Global Foundires); Janice Golda (Intel); Bill Rozich (Albany/IBM); Sima Salamata (TI); Kevin Logue (TI); Sitaram Arkalgud (SEMATECH); Hans Stork (AMAT); Paul Edstrom (GE); Jean LeMoin (MCA); and independent consultants Bill Tobey, Ken Rygler, and Takeshi Hattori.

The ConFab presented a nice balance of economic data and forecasts with technical topics, such as EUV vs nanoimprint lithography, the cost of test, 3D integration, and other trends.

These were the times when it felt that the economy was at the edge of an abyss and our discussions often turned to "will this all be over in June or should it be the overarching theme of the conference?" The semiconductor industry is still climbing out of that deep dark hole, but it now seems safe to say the worst is over. In the end, the conference presented a nice balance of economic data and forecasts with meaty technical topics, such as EUV vs nanoimprint lithography, the cost of test, 3D integration, as well as practical discussions of how to extend fab longevity. For the first time, we also covered the convergence of the semiconductor and solar industries and how photovoltaics technology was evolving.

Keynote speaker Brian Krzanich, Intel's VP and GM of manufacturing and supply chain, gave everyone a smile to start, sharing research that shows that people are willing to give up about anything before they would give up broadband Internet, including toiletries, clothing and even food. It doesn't say much about society, but it does mean the Internet and its required infrastructure are here to stay.

Bill McClean of IC Insights further amplified that the demand for semiconductors remains strong, noting that a quarter billion cell phones were shipped in the second quarter. "From the industry's tone, you would have thought it fell to zero," he said. He noted that the industry had not added capacity to keep up with underlying demand so he is predicting "boom" years of double digital growth in 2010 and 2011. Historically, that has always been the case. Every recession in the past, without fail, has been followed by strong semiconductor growth.

George Scalise, president of the Semiconductor Industry Association shared similar views on the industry's long term prospects, noting that semiconductors are the 2nd largest export from the U.S. (behind only oil refinery products). Scalise noted that, according to a recent study, semiconductors are now the driving force behind U.S. energy efficiency gains (www.aceee.org/press/e094pr.htm). The study reports that the need for 184 electric power plants has already eliminated due to more efficient semiconductor technologies, and that $1.3 trillion in reduced electric bills is seen over the next 20 years.

The great debate at the conference was over what lithography approach will supersede the existing approach (ArF immersion with double patterning). The two technologies presented as viable approaches: EUV lithography and nanoimprint. EUV came out as the clear winner with good progress reported by Nikon and Toppan. However, it was also clear that massive amount of investments and technical advances were still required for either to be truly workable in high volume manufacturing. What's missing is advanced mask inspection tools for EUV and fast e-beam writing tools for NIL: both will require millions in investment, yet little work has been done.

The cost of test panel carried something of a surprise. Gone are the days of million dollar test systems. Today's systems are more in the $200K range, thanks to design for test (DFT) and built-in self-test (BIST) strategies. The real test challenge may lie in 3D integration: there is simply no way to access all those little vias post-stacking to make sure they're good. Could be a show stopper. Solar? Dan Hutcheson showed a chart where a tiny area in the middle of Africa could power the entire world. It's definitely the future of energy. ■

Pete Singer
Editor-in-Chief

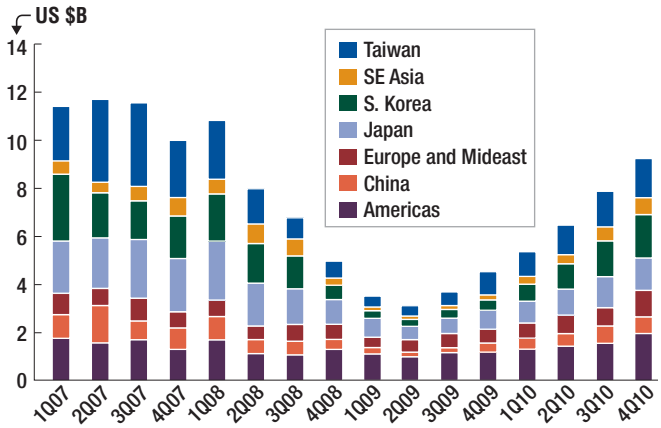
WORLD NEWS

BUSINESS TRENDS

SEMI: Fab investments poised for a comeback

Fab spending has been sliding since early 2008 and is poised to sink to a 10-year low in 2009, according to recent data and projections from SEMI—but the good news is that 2010 could see a 90% surge in fab investments.

After tailing off as early as 1Q08, investments in frontend facilities (construction and equipment) quickly fell through the floor, according to SEMI; the group pegs a projected -51% decline for all of 2009 vs. 2008, and the pace of facilities closures will nearly double (35 vs. 19). Worldwide capacity will decline about 3% overall to 15M wafers/month (200mm equivalent), and twice that rate of decline (-5% to -7%) for the much-maligned memory sector.



Investments in front-end facilities, construction + equipping. (Source: SEMI World Fab Database)

However, looking at the quarterly picture, we could now be at the bottom of the trough. SEMI anticipates investments in fab projects and equipment will ramp up in 2H09 and into 2010, and through 2010 fab investments could be nearly double (+90%) anticipated levels for this year. Activity in the Americas is notable, mainly thanks to Intel's 32nm ramp (now ongoing) and GlobalFoundries proposed fab in Malta, NY (construction starting in mid-2009). Also note the total evaporation of investments in Asia, particularly Taiwan and Korea (which are heavily memory).

Several new fabs are expected to begin construction in 2009, according to a related report from Christian Gregor Dieseldorff of SEMI Industry Research and Statistics—three in Europe/Mideast/Russia, and two in the Americas, including GlobalFoundries which is the lone high-volume fab. As many as nine facilities will also commence operations (spanning the Americas, China, Japan, Taiwan, and Europe/Middle East); six are 150mm and below, with three 200mm and a single 300mm fab. Also, three of this group are foundries, two are at universities, and the rest are for MEMS/discretes.

WORLDWIDE HIGHLIGHTS

After a -34% plunge in silicon wafer demand in 1Q09, demand spiked ~50% in 2Q as suppliers quickly rebuilt inventories they slashed earlier back to normal levels, according to Gartner—but the firm's still wary of broader demand for device production until after 3Q09.

Toshiba and **NEC** are deepening ties with the **IBM**-led Common Platform Alliance to high-*k*/metal gate LSI at the 28nm node.

Suss MicroTec and **3M** are partnering to configure their technologies for temporary bonding of ultrathin wafers for 3D packaging.

Wolfgang Mueller, who spearheaded development of **Qimonda**'s "buried wordline" and 4F(2) bit cell DRAM technologies, has been hired by Z-RAM memory firm **Innovative Silicon Inc.** (ISi) to work on their sub-40nm process technologies.

USA

Applied Materials has handed over most of its stake in **Sokudo**, its coating/development track tool JV, to partner **Dainippon Screen**.

Novellus says it has developed dense ultralow-*k* materials for 32nm integration, with 5% lower k_{eff} combined with the company's diffusion barrier layers.

GlobalFoundries has hired two ex-Applied Materials and **AMD** execs to head up its Fab 2 in upstate New York. It also has demonstrated a technique that allows equivalent oxide thickness (EOT) in a HK+MG transistor to scale beyond the level required for the 22nm node.

Cadence Design Systems says it is laying off about 5% of its workforce and reducing investments in what it calls "the manufacturing side" of design-for-manufacturing (DFM).

Nanometrics has purchased inventory and other assets of **Zygo**'s chip tool business, notably its Unifire line of products.

RF Micro Devices has formed a gallium nitride (GaN) foundry services business unit, targeting "multiple RF power markets."

Aviza Technology has filed a voluntary Chapter 11, and will sell some assets to **Sumitomo Precision Products**.

ASIAFOCUS

Toshiba has devised a gate stack with an added strontium germanium interlayer to achieve the high carrier mobility required for 16nm LSIs. The company also reportedly has a new simulation tool that helps boost 40nm chip yields.

TSMC has reappointed chairman Morris Chang as CEO, to help push outside the semiconductor world into LEDs and solar energy.

Local reports quote **Intel** execs indicate the chipmaker's 300mm fab in Dalian, China, will open in 2010 using 65nm process technologies.

AU Optronics plans to purchase a majority stake in Japanese poly-Si supplier **M.Setek**.

UMC shareholders have given the green-light to the foundry's proposed $285M takeover of mainland partner **HeJian Technology** (Suzhou).

Citing sluggish demand, **Panasonic** is mulling a delay in opening its new ¥94B image sensor chip plant in Toyama Prefecture, which it announced in Jan. 2008. Meanwhile, Toshiba reportedly will convert its Kitakyushu plant to optical device production, possibly with new equipment investments.

Dai Nippon Printing says it has designed a lead frame for that uses only a third the normal amount of gold wire, and reduces chip package costs by around 40%.

Yingli Green Energy, **Tempress Systems**, and the Energy Research Centre of the Netherlands are forming a research collaboration to develop high-efficiency N-type silicon solar cells.

EUROFOCUS

Peter Wolters has devised new sensor and process control capabilities for its double-sided wafer polishing systems that meet 22nm lithography requirements.

Soitec says its 300mm ultra-thin SOI wafer platform is qualified and ready to support the 22nm node and beyond.

ASMI is divesting its Levitor rapid thermal processing (RTP) business in a management buyout, but will hold a minority stake.

X-Fab is offering its first foundry process for Hall sensors in 0.18µm process technology.

Alchimer says its improved eG ViaCoat wet deposition process for copper (Cu) seed TSV provides up to 80% cost savings versus dry vacuum processes. ■

TECHNOLOGY NEWS

Intel Research Day: Update on EUV, other projects

Research at Intel Labs covered at the chipmaker's annual event (June 18, Mountain View, CA) covered the major categories of eco-innovation, 3D graphics on the Internet, mobility, and enterprise. But Mike Mayberry, VP technology & manufacturing group director of components research, conducted a roundtable discussion that focused on the company's manufacturing research, including a summary of the status of EUV.

Not surprisingly, Mayberry noted that EUV source technology is probably the most critical path item. In the "first wave" of tools (those used for R&D) so far, one of the beta sources can run a tool at ~10 wafers/hr, and has been run in burst mode at about 5X that speed, but has not yet proven that it can run a full year with only routine maintenance; also, the current class of scanners is running at ~1wph. The "second wave" of tools (for development) is expected to begin arriving next year. "So in principle, if you start development next year and it took two to three years to do development, that would place production in the 2012-2013 timeframe," he said. Then a "third wave" of production tools would be required, though Mayberry would not speculate on how close together the second and third waves might turn out to be.

Intel has printed features down to 24nm using EUV, but it also knows how to extend 193nm down to that point by adding extra masks and extra cost to the wafer. "At some point they [193nm immersion and EUV] will cross over, so the world will not end if EUV is not ready by the time we get to this point," Mayberry said, adding that various cost analyses suggest a cross-over point for memory just below the 32nm node.

The company can print features at ~35-40nm with one mask layer using 193nm immersion, and can go even smaller by employing "tricks" such as "doubling up on the masks," Mayberry explained. "We can do other forms of adding information to the wafer that you can't get through the optical system—so there are alternatives where you can go smaller." Intel also has a lab demo setup that can print features (lines and spaces) at 15nm with 193nm litho, "but you can't make a useful pattern with it in a single step," he noted. So there are alternatives to EUV, but not necessarily better (if EUV is working as anticipated).

Regarding metals for interconnects, Mayberry explained that when the industry gets down to a 10nm wire, scattering around the surface will be the dominant effect. "We are weighing various options, such as how to engineer the surface, as well as the interaction between materials," he said. "We'll continue to push copper for a long time—but we're already weighing alternatives to that so they're ready when we need it."

As usual, the familiar question about the end of Moore's Law (and the implications if only one company can afford to stay on its path) came up during the roundtable. "People have been predicting the end of Moore's Law for a long time...consolidation has obviously happened, but it's always been slower and more unpredictable than people would have guessed," explained Mayberry. He hesitated to predict how fast the consolidation will take place and who the winners will be, though he thinks Intel will be among that group. — ***D.V.***

Applied targets 22nm copper barrier/seed PVD

Applied Materials says its new Endura CuBS RFX PVD system, qualified for copper barrier/seed deposition technology at 32nm and 22nm for production of logic and flash memory, provides a lower cost/wafer than competing technologies, including CVD alternatives, by as much as 40%—calculating a normalized COO of the 130Å Ta + 450Å RFX Cu process (CuBS) at $1/wafer, according to Marek Radko, the firm's BEOL GPM manager.

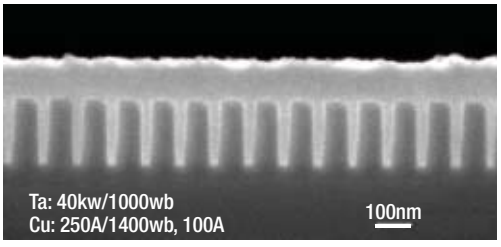


Figure 1. Gap fill on 2x node trench. (Source: Applied Materials)

Effective barrier and seed layer deposition is critical to assuring the speed and reliability of copper interconnects as it prevents copper diffusion and provides a quality nucleation layer for subsequent bulk copper fill. The main issues with copper gap fill at 32/22nm, Radko told *SST*, are overhang and sidewall coverage, along with asymmetry at the wafer's edge. There are three key considerations for the new process technology: a flux optimizer, universal magnet motion (UMM), and high-energy copper ion resputter (ratio of ions falling on the wafer vs. ions/atoms redistributed inside the feature).

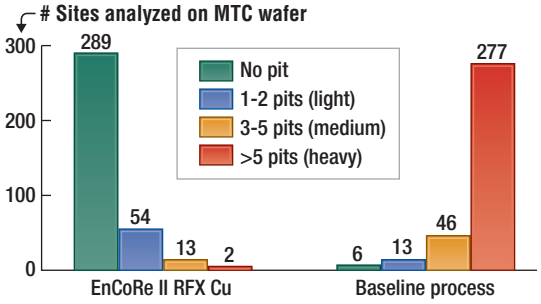


Figure 2. Post-CMP data (MTC trench: 25nm). (Source: Applied Materials)

The flux optimizer, made of copper and positioned between the target and the wafer, acts as a kind of directional lens for the ions. By improving the directionality of the ions, bottom coverage is improved and overhang minimized. When the flux optimizer is used in conjunction with the

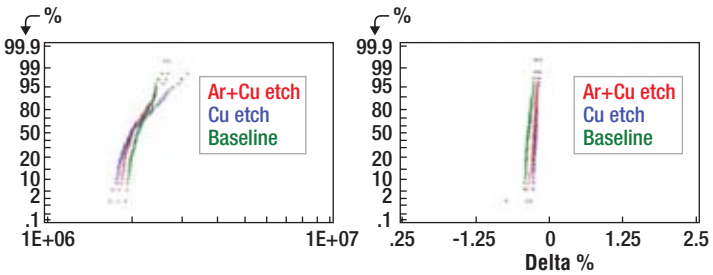


Figure 3. Top: Long via-chain RC (1.38M vias). Bottom: SM 168hr/250C (1.38M vias) (Source: Applied Materials)

UMM—the new magnet design, a multi-directional magnet that allows movement up and down—the entire surface area of the target can be used and compensation for target erosion is achieved, Radko explained. (The angle of ion deposition in the new chamber design is not distorted to the extent it is in conventional technologies). Furthermore, the flux optimizer minimizes the area where plasma condensation occurs; the plasma is directed to an area right above the wafer. Optimized magnetron trajectories in the UMM change the wear pattern; the tool operator can multiplex different types of motions of the magnet.

"With the baseline process, i.e., a straight, directional copper ion deposition, the process window was very small and the bias and resputter ratio were very small," said Radko. "As we increased the resputter ratio, we found a regime where the process window is very large and all aspects of good deposition—sidewall coverage, bottom coverage, and top opening—are extremely compatible with ECP without defects and voids."

The company believes it has an advantage in this application sector because the technology has been production-proven over the years (the original Endura CuBS PVD tool was launched in 1997), making it less risky for chip manufacturers to introduce. Furthermore, the new process is extendable to the next two nodes. — ***D.V.***

GA Tech: Graphene could replace Cu for IC interconnects

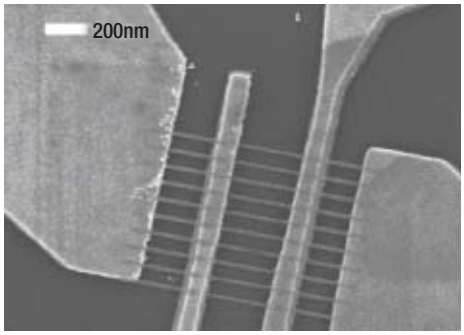
Researchers at Georgia Tech say they have experimentally demonstrated the potential for graphene to replace copper for on-chip interconnects and help extend performance scaling for silicon-based ICs.

Their work, published in the June 2009 issue of the IEEE journal *Electron Device Letters*, shows resistivity in graphene nanoribbon (GNR) interconnects as narrow as 18nm, "comparable to even the most optimistic projections for copper interconnects at that scale," and "probably already out-perform copper at this size scale," according to Raghunath Murali, a research engineer in Georgia Tech's Microelectronics Research Center, in a statement.

A key problem with copper interconnects is that at nanoscale-dimensions conductance is affected by scattering at the grain boundaries and sidewalls, Murali explained. "These add up to increased resistivity, which nearly doubles as the interconnect sizes shrink to

 continued from page 7

30nm." At the ~20nm scale the increased resistance would offset performance increases and negates gains made in higher density—a roadblock to performance increases, if not to actual scaling, he noted. "We would be giving up so much in terms of resistivity, we wouldn't get a performance advantage," he said. And thus, the search for evaluating different materials for interconnects.



SEM image showing 22nm wide graphene nanoribbons between the middle electrode pair. (Source: Georgia Tech/ Raghunath Murali)

In their work (Murali, Kevin Brenner, Yinxiao Yang, Thomas Beck, and James Meindl), flakes of multilayered graphene were removed from a block and placed in an oxidized silicon substrate; on that they constructed four electrode contacts using e-beam lithography, and then devices with parallel 18-52nm wide nanoribbons. 3D resistivity of the nanoribbons on 18 different devices was measured using standard analytical techniques at room temperature. Results indicated the best GNRs possessed conductivity equal to that predicted for Cu interconnects at the same size. Average resistivity at a given linewidth was found to be about 3× that of a Cu wire; the best GNR had a resistivity comparable to Cu.

From the paper abstract:

The conductivity is found to be limited by impurity scattering as well as line-edge roughness scattering; as a result, the best reported GNR resistivity is three times the limit imposed by substrate phonon scattering. This letter reveals that even moderate-quality graphene nanowires have the potential to outperform Cu for use as on-chip interconnects.

Moreover, they say, the comparison was between "non-optimized" graphene and "optimistic estimates" for Cu, and without using "especially clean processes." A key property of graphene is its ballistic transport (low resistance), but the researchers noted that actual conductance is limited by scattering from impurities, line-edge roughness, and substrate phonons (vibrations in the substrate lattice). "With our straightforward processing, we are getting graphene interconnects that are essentially comparable to copper," noted Murali. "If we do this more optimally, the performance should surpass copper."

The research was supported by the Interconnect Focus Center (one of the Semiconductor Research Corp./DARPA Focus Centers) and the SRC's Nanoelectronics Research Initiative through its Institute for Nanoelectronics Discovery and Exploration (INDEX). — ***J.M.***

Oerlikon discusses path to $0.70/W thin-film PV panels

Oerlikon Solar announced during this spring's Intersolar in Munich that it had achieved 11% initial power conversion efficiency on its full-size micromorph (a thin-film technology) modules (1.4m^2), or 151Watts of initial power. That news, along with unbridled optimism about the future of crystalline silicon (c-Si) exhibited at the recent Intertech-Pira Photovoltaics Summit, provided the backdrop for an interview with Oerlikon's Chris O'Brien, head of market development, North America.

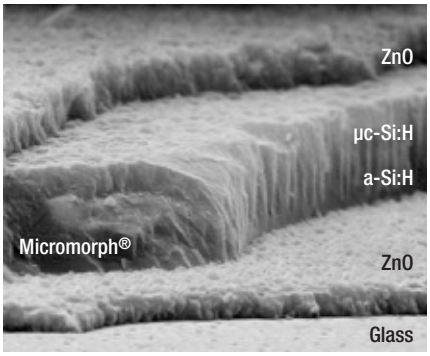
The company says its micromorph technology boosts solar-cell efficiency by adding a second microcrystalline absorber to the amorphous silicon (a-Si) layer, which converts the energy of the red and near-infrared spectrum, facilitating efficiency increases of up to 50%. The company ran a batch of five full-sized modules through its pilot line in Switzerland, using the same manufacturing process and materials already in use by the company's end-users. The initial 11% efficiency will probably stabilize to ~9.7% on those five modules, O'Brien told *SST*, but "what was encouraging about the results is that the absolute number was a significant boost over what we're guaranteeing today [and] the spread among the modules was quite tight [3W]—so that gives us confidence that this is a replicable result."

Based on data from 10 identified end-users, Oerlikon is on track to meet its roadmap goal whereby end-users will be able to produce panels at a cost of $0.70/W by the end of 2010, O'Brien said—a cost that the company believes will put end-users in a competitive position with respect to the broader renewables market, and would allow delivery of solar-generated electricity at a price of ~$0.09/kW-hr for one large scale project currently being developed in California, "a very competitive price in the large wholesale markets," O'Brien noted. To meet its roadmap goal, the company is continuing to improve efficiency in its micromorph technology, and improve its manufacturing process (e.g., throughput, yield, etc.). By the end of 2009, after two years selling its end-to-end solution, it will have 600MW cumulative capacity installed at different sites in Europe and Asia, he said.

O'Brien also addressed the points frequently being discussed at technical conferences—i.e., grid parity—and the seeming concurrence among industry insiders of a constant 80%/20% split (or maybe 70%/30%) of market share that favors c-Si over thin-film PV. "There's so much interest in thin-film technologies in general because they have dramatically simpler manufacturing steps and use much less material when making a module compared with c-Si," explained O'Brien. For its part, Oerlikon expects thin-film "will grow to at least 25% of market share by 2012," he said. "There will continue to be a strong market for c-Si, but the fastest growth will be in thin-film technologies because of inherent cost advantages."

Regarding grid parity, O'Brien thinks it's a simplistic notion. "Delivering energy value is one part of the equation, but there are many other factors," he noted, including access to electricity transmission and policies supporting simple grid interconnection. "A pre-requisite to that happening is reaching a value point where solar is competitive effectively against the other peak energy alternatives."

In summary, O'Brien believes that the overall PV markets will increase and thin-film will need to deliver on its technology roadmap, and he disputes the market share pessimism. "When thin-film gets to $0.70/W, it will get a larger share of the market," he said, suggesting that there is a very large market for any solar tech that can deliver electricity in the $0.10-0.12/kW-hr range. "We have a clear path to this point," he added, whereas "it's not as clear to me that c-Si has a clear pathway to that same operating point on a sustainable basis." — ***D.V.***



Micromorph thin-film cell cross-section. (Source: Oerlikon Solar)

COMPONENTS AND SUBSYSTEMS/
ION IMPLANT

COVER ARTICLE

New regs on sub-atmospheric gas sources reduce risk, improve safety

EXECUTIVE OVERVIEW Ion implant has traditionally been hazardous due to the toxic materials and high-pressure cylinders. However, sub-atmospheric gas sources (SAGs) have been proven to help improve safety. Due to the growing adoption of SAGs, the National Fire Protection Association (NFPA) recently published definitions and guidelines for their use. This article describes the two primary types of SAGs and their differences as they relate to safety and efficacy.

Historically, ion implant has been considered a hazardous area in a semiconductor fab. As recently as 15 years ago, implanters were isolated in a corner of the facility to minimize potential exposure to the toxic gases used during implant. High-pressure cylinders located in a confined area inside the implanter presented a challenge for semiconductor manufacturers.

Over the years, the semiconductor industry learned to prepare for and prevent gas leaks. Strategies to control the risk include source isolation, ventilation, gas-detector technology, improved gas delivery components and systems, and extensive personnel training. It is also common to install treatment systems designed to prevent discharges-to-atmosphere above allowable limits.

The introduction of sub-atmospheric pressure gas sources (SAGs) in the mid-1990s enabled semiconductor manufacturers to overcome the risk posed by hazardous materials inside the tool. Environmental health & safety (EHS) professionals, insurance underwriters, and loss control engineers endorsed the potential safety benefits of SAGs.

Fabs under pressure

Strategies emerged to reduce the risk inherent in using highly toxic gases for ion implantation. One involved removing pressure from the system; without pressure, there is no release driver. The second uses embedded mechanical controls to mitigate cylinder pressure. Both require a vacuum to be in place before gas is delivered from the cylinder to the tool. Recently, NFPA published definitions of these two approaches and recommendations for their use. Here, we explore recently released standards that establish and define Type 1 and Type 2 SAGs and examine adoption trends and safety/economic benefits.

NFPA 318 defines SAG types

Adopting new technology involves many groups: end-users/engineers, the ESH and fire service communities, and risk underwriters. Given the divergence in the underlying technologies used to achieve sub-atmospheric pressure delivery, adopting code language that governs their use has been challenging.

The terms Type 1 and Type 2 were established in late 2008, when NFPA 318 approved a dual definition [3.3.28.5.1-2] to differentiate SAGs based on gas-storage pressure. The 2009 edition provides the following definitions:

- 3.3.28.5.1 Sub-atmospheric Gas Storage and Delivery System (Type 1 SAGs). A gas source package that stores and delivers gas at sub-atmospheric pressure and includes a container (e.g., gas cylinder and outlet valve) that stores and delivers gas at a pressure of less than 14.7 psia at NTP.
- 3.3.28.5.2 Sub-atmospheric Gas Delivery System (Type 2 SAGs). A gas source package that stores compressed gas and delivers gas sub-atmospherically and includes a container (e.g., gas cylinder and outlet valve) that stores gas at a pressure greater than 14.7 psia at NTP and delivers gas at a pressure of less than 14.7 psia at NTP.

While both types of systems reduce the risk of using highly toxic gases in ion implanters, there are some fundamental differences.

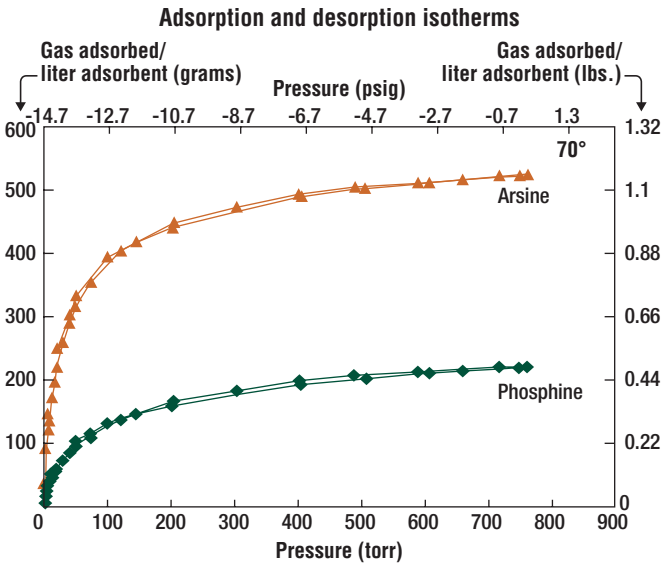


Figure 1. Arsine and phosphine adsorption isotherms on high-density carbon at 70°F.

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Type 1 sub-atmospheric gas sources

The first SAGs operated by reversibly adsorbing dopant gases within a high surface area carbon matrix (**Fig. 1**). The adsorbed gas, in a lower energy state, exhibits a significant vapor-pressure reduction. With surface areas of 1200m^2/gr, sorbent loadings (the saturation of gas into the sorbent) of 30–50% by weight can be stored at a final pressure of 650torr at 20°C. A vacuum, afforded by the process, provides the motive force to displace the gas/solid equilibrium and convey the gas to the point of use.

Removing the pressure component effectively eliminated the prospect of accidental gas leaks from this SAG type, allowing semiconductor facilities to move away from inefficient solids vaporization and standardize on 100% pure gases. Results include greater process throughput and reduced operating and capital costs. The term gas source was coined to describe the new sub-atmospheric pressure delivery methodology.

In 1999, industrial property insurer FM Global, recognizing the inherent risk reduction offered by SAGs, modified its Property Loss Prevention Guide for Semiconductor Facilities (Data Sheet 7-7), to advocate "the use of sub-atmospheric gas sources instead of high-pressure cylinders whenever process compatibility will allow."

Over 130,000 Type 1 SAGs have been deployed for use within the semiconductor industry, with no reported safety incidents. The science behind Type 1 SAGs has continued to evolve and improve; most recently, advancements in sorbent technology have doubled delivery capacities, helping reduce cylinder change-out frequency.

Type 2 sub-atmospheric gas sources

Over the past 15 years, alternative dopant packaging technologies have also been developed. Examples include on-demand gas generators and vacuum-initiated cylinders. The latter uses pressure-control devices embedded within a traditional compressed gas cylinder, effectively transforming it into a smarter and safer gas delivery vessel. NFPA now refers to these cylinders as Type 2 SAGs.

High-pressure cylinders delivering their contents at sub-atmospheric pressure began appearing after 2002. With a focus on vacuum-initiated delivery, these new cylinders were configured to permit flow when a minimum threshold pressure was achieved. In this manner, a cylinder at 200–1500psig discharges its contents when the downstream manifold is under vacuum (<760torr). If a pre-set threshold vacuum is not maintained, an internal valve will close. Maximum discharge rates are capped using restricted flow orifices or other flow-restricting means. As with Type 1 SAGs, the process provides the negative operating pressure required to activate the internal regulator.

While, in theory, pressure-control devices could be located downstream of the cylinder valve, they are typically located inside the cylinder of today's Type 2 SAGs. These cylinders also feature separate fill and discharge ports. Locating the mechanical devices within the cylinder minimizes the possibility of damage or tampering, but increases the premium on reliability. Servicing the internal components is virtually impossible given their location. Long-term reliability and sustainability of SAGs with embedded internals is being established. Certainly this delivery concept offers some notable benefits in adapting sub-atmospheric pressure delivery to a broad variety of gases. At present, there is a fleet of ~6,000 Type 2 SAGs deployed for use within the semiconductor industry.

Fire survivability differences

Recent fire testing demonstrated that during exposure to low- to intermediate-temperature fires — temperature exposures that could foreseeably occur during a storage fire — Type 1 cylinders survived significantly longer than Type 2s. In addition, the pressure wave generated during cylinder failure was significantly less on a Type 1 system.

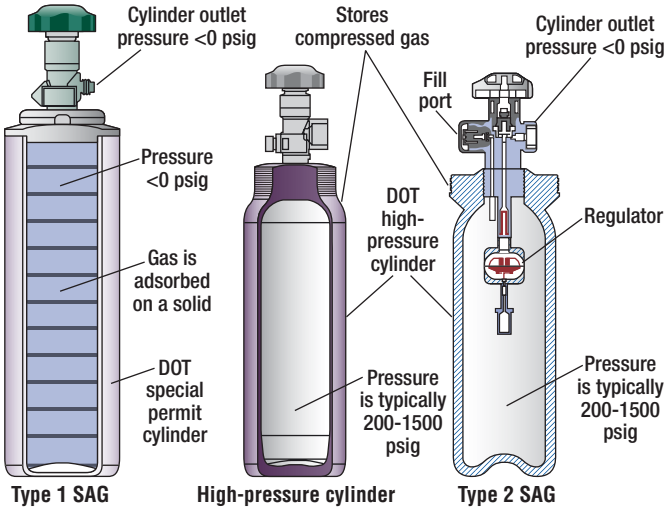

Figure 2. Typical container configurations for Type 1 and Type 2 SAGs and traditional high-pressure cylinders.

Benefits derived from safer packaging

An immediate benefit of safer gas packaging is that users can increase the quantity of dopant stored in the implanter. Larger cylinders and increased fill densities translate into greater production efficiencies by reducing the frequency of cylinder change-outs. At present, Type 2 SAGs provide greater capacity for liquefied compressed gases.

The absence of pressure in Type 1 SAGs facilitates additional operational cost savings. While Type 2 SAGs can also achieve some or all of these benefits, it comes with additional engineering controls.

Components and subsystems continued from page 11

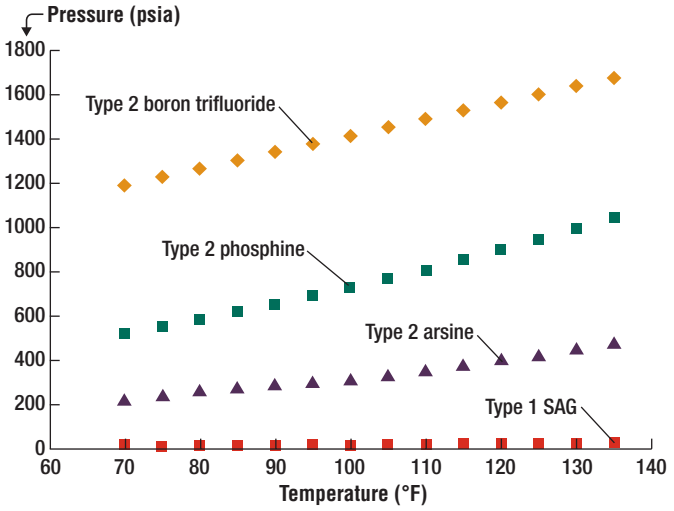

Figure 3. Typical dopant pressures for Type 1 and Type 2 containers from 70°–130°F.

Inherent benefits of Type 1 SAGs

Designating performance-based control methods helps ensure that the gas delivery is always at sub-atmospheric pressure. FM Global's Property Loss Prevention Data Sheet 7-7 states: "Provide sub-atmospheric pressure cylinders with a pressure sensor designed to shut off the cylinder if the [delivery] pressure exceeds 1 atmosphere [760 torr]." Type 1 SAGs provide this condition inherently.

Stored pressure within Type 2 SAGs creates the potential to release the entire gas inventory into the atmosphere, though this is rare. NFPA 318 advises an emergency high-pressure shutoff be provided after the

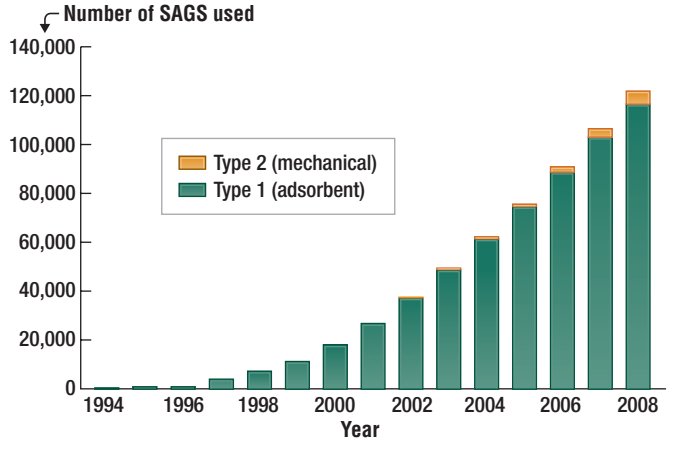

Figure 4. Cumulative Type 1 and Type 2 SAG usage since introduction in 1994.

SAG Type 2 cylinder to protect the gas distribution system. Current standards on gas-box ventilation are based on anticipated worst-case release (WCR) rates. Given the very low WCR rates for Type 1 SAGs, reductions in implanter gas-box exhaust rates can be large: an estimated energy savings of $1,200–1,500 per tool, per year.

Opportunities for savings include reclassification of gas-box exhaust from "scrubbed" to "general exhaust" and/or eliminating treatment systems altogether. For new facilities, this will reduce ductwork and associated make-up air units. Given the lower risk profile of Type 1 SAGs, the level and frequency of toxic-gas monitoring can be re-examined and possibly reduced.

Conclusion

Today, implanters are installed in the center of the fab, reflecting their critical role in semiconductor manufacturing and the quantum leap of safety improvements in dopant delivery packaging.

Recognizing SAG types in the codes helps ensure the maximum benefit from lower-risk technologies. As code officials consider design alternatives, inclusion of specific language accurately defining SAGs and their types ensures uniform application and understanding.

Aside from implanter efficiency gains, the industry can obtain additional savings from lower-cost gas boxes and components, reduced exhaust rates, and smaller ductwork. Some of the investment

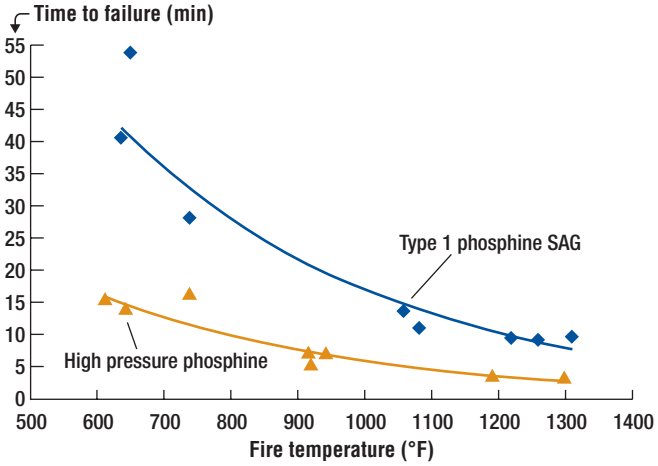

Figure 5. Comparison of type 1 and high-pressure phosphine cylinder survivability under simulated fire conditions.

historically required to prevent and contain gas releases can be avoided in the future.

Sub-atmospheric pressure gas delivery offers real safety and risk reduction benefits. With a proven 15-year service history, Type 1 SAGs have moved the industry toward inherent safety and virtually eliminated the prospect of a catastrophic event. During the next 5-year period, critical reliability data will better characterize the relative risk benefit between Type 1 and Type 2 SAGs.

Given the general concern about safety with highly toxic materials in transport and use, SAG adoption will grow. ■

Acknowledgments

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THERMAL PROCESSING

Thermal processing issues for 22nm node junction scaling

EXECUTIVE OVERVIEW Junction scaling for 22nm node planar and FinFET CMOS requires low energy implantation, but the surface oxide thickness will determine the energy (>83eV) and dose. Engineering the surface amorphous layer maximizes dopant activation, and reduces implant damage and junction leakage with sub-melt laser or flash lamp annealing. The annealing process and equipment must be optimized to prevent strain relaxation, high-*k*/metal gate stack failure and wafer breakage.

A main focus with junction scaling for the 22nm node is defect reduction and lowering junction leakage, especially for system on a chip (SOC) with logic embedded memory devices. There are several ways to reduce residual implant damage from an implant and annealing perspective. Low damage implantation can be realized by: 1) higher implant beam current or dose rate; 2) lower implant wafer temperature (cryo-implantation) 0°C to -160°C by using chilled water or liquid nitrogen wafer cooling; 3) using molecular dopants such as $B_{18}H_{22}$, $B_{36}H_{44}$, As_4 or P_4; and 4) using lower dose heavier ions for pre-amorphizing implant (PAI) such as In, Sb, or Xe. These techniques improve self-amorphization, lower critical implant doses for amorphization and smooth amorphous interfaces thereby reducing end of range (EOR) and residual implant damage while enhancing dopant activation with msec anneal (MSA). Higher MSA peak temperature and/or pre-/post-MSA diffusionless spike/RTA at <900°C leads to stable defects and a reduction in residual implant damage, improving junction leakage.

Planar CMOS doping

At the 22nm node, dopant diffusion must be minimal to achieve the targeted junction depth (X_j) between 6 and 12nm. The three options for doping these ultra-shallow junctions (USJ) are: 1) lower energy beam-line implantation without deceleration energy contamination, 2) higher energy beam-line implantation using molecular dopants, or 3) plasma implantation. For p+ USJ, monomer B >83eV or BF_2 >450eV implant energy with no dopant channeling, and for maximum dopant activation and low leakage Ge-PAI >3keV, Xe-PAI >5keV, or In-PAI >5keV. Using $B_{18}H_{22}$ (>2keV) or $B_{36}H_{44}$ (>4keV) molecular dopants avoids the need for PAI due to enhanced self-amorphization, but retained dose is only 75%; 55% with BF_2. **Figure 1** shows high-depth resolution PCOR-SIMS of 100eV B equivalent at 1E15/cm^2 dose for $B_{18}H_{22}$ and $B_{36}H_{44}$ implantation into crystalline and amorphous silicon using the Nissin Claris molecular dopant implanter [1]. Note that the difference in X_j at 5E18/cm^3 with and without Ge-PAI is only 0.4nm (X_j=7.2nm versus 6.8nm) due to the self-amorphization effects of molecular dopants.

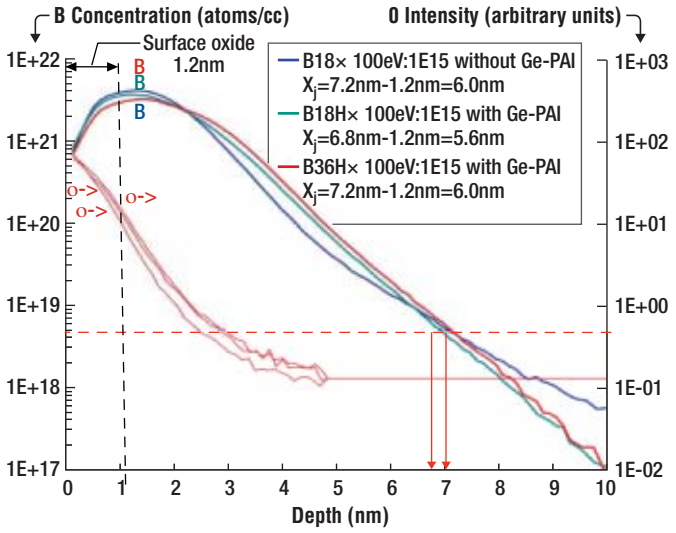

Figure 1. B dopant profile and surface oxide profile using PCOR-SIMS for $B_{18}H_{22}$ and $B_{36}H_{44}$ at 100eV equivalent and 1E15/cm^2 total dose [1].

With PCOR-SIMS, the presence of a 1.2nm-thick surface oxide was detected as shown in Fig.1, so the corrected electrical B junction depths are 6.0 and 5.6nm, which becomes critical for process and device simulation modeling when the surface oxide can be 20-30% of the physical implant depth and contain 40-60% of the total dose. Without this surface oxide, the implant energy would need to be reduced from 100eV to 83eV to achieve an X_j<6nm. With BF_3 plasma implantation (>250V), an amorphous layer (PAI) is still required to reduce channeling and enhance dopant activation, but a major problem is surface sputtering and retained dose of <11% [2]. This can be improved if using B_2H_6+He plasma implant process. For n+ extension switching from arsenic (As) to phosphorus (P) or antimony (Sb) at 500eV or 1.7keV, respectively, improves dopant activation with MSA, and the lateral straggle with P improves gate overlap with 0° tilt angle, avoiding the need for tilted nSDE implan-

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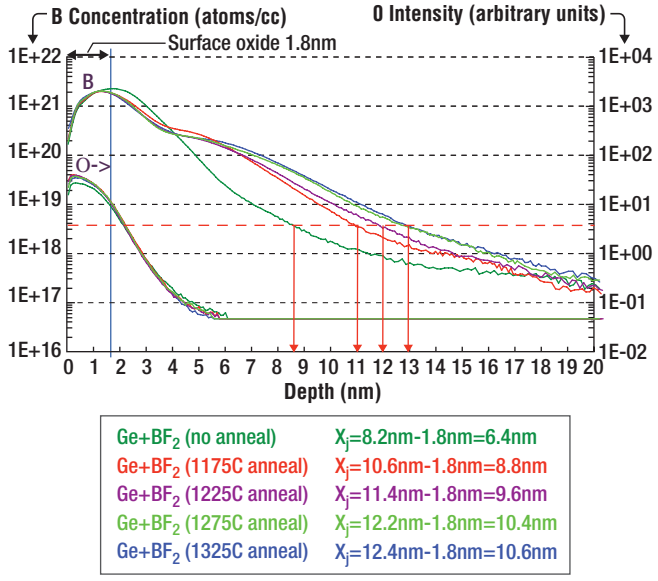

Figure 2. B dopant profile and surface oxide profile using PCOR-SIMS for Ge+BF_2.

tation when using As or Sb dopant species.

Achieving shallow as-implanted X_j does not guarantee USJ after MSA, where as much as 4nm of dopant diffusion can occur due to diffusion during amorphous layer regrowth, especially when using PAI. PCOR-SIMS of B and surface oxide for 10keV Ge-PAI at 5E14/cm^2 and 500eV BF_2 at 1E15/cm^2 implantation on the AIBT iPulsar single wafer high-current implanter followed by MSA on the Applied Materials DSA sub-melt laser annealer at 1175°C, 1225°C, 1275°C, and 1325°C is shown in **Fig.2**. Compared to the no-annealed reference, 1175°C anneal resulted in 2.4nm of B dopant movement; this increases to 3.2nm at 1225°C, 4.0nm at 1275°C, and 4.2nm at 1325°C. The sheet resistances (R_s) reported in ref. 2 were 2000 Ω/sq. for 1175°C and 1225°C, 1800 Ω/sq. for 1275°C and 1400 Ω/sq. for 1325°C. The corrected electrical X_j was determined by subtracting out the 1.8nm surface oxide thickness detected by PCOR-SIMS, so the calculated B dopant activation level limited by boron solid solubility (B_{ss}) varied from 6 to 8E19/cm^3 as shown in the R_s versus X_j chart of **Fig. 3**.

Without Ge-PAI, the corrected X_j for BF_2 with 1325°C MSA was 6.6nm for a B_{ss}=4E19/cm^3 whereas with 1175°C MSA, X_j was 5.8nm for a B_{ss}=3E19/cm^3 (Fig.3). Due to the lower retained dose with BF_2 (5.5E14/cm^2) the maximum dopant activation was much lower than the monomer B results. The surface oxide for all the monomer B implants was thicker at 2.3nm based on PCOR-SIMS and verified by XPS and X-TEM [2]. The corrected electrical X_j after the 1325°C MSA for B was 6.9nm, Ge+B was 10.5nm, and Xe+B was 9.7nm. The B_{ss} values for the monomer B implants shown in Fig.3 are: 1) B_{ss}=5E19/cm^3 for 1175°C and 1225°C MSA, 2) increases to B_{ss}=1.2E20/cm^3 for 1325°C MSA, 3) increases to B_{ss}=1.3E20/cm^3 with Ge-PAI at 1325°C MSA, and 4) up to B_{ss}=3.5E20/cm^3 with Xe-PAI at 1325°C MSA.

Reducing residual implant damage or EOR defects and junction leakage current can also be achieved by using higher MSA temperatures, additional pre- or post-MSA 900°C spike/RTA or low damage PAI as shown in **Fig.4**. Similar RsL leakage results for monomer B and BF_2 were reported in ref. 3. A 14–16nm deep amorphous layer is created by the Ge (10keV), Xe (14keV) and In (14keV) PAI. The lowest junction leakage <5E-8A/cm^2 is realized for In-PAI, while for Ge-PAI the leakage is in the E-5A/cm^2 level for 1175°C MSA temperature and improves to E-8A/cm^2 level for >1275°C. Xe-PAI behaves differently; the leakage level is E-4A/cm^2 for all MSA temperatures but a pre-MSA 900°C spike/RTA improves leakage to E-6A/cm^2 level. Reducing the Xe-PAI energy to 5keV will reduce the amorphous depth to <6nm (X_j-EOR=+nm) and leakage to <E-7A/cm^2 level as reported by Borland et al. using Si-PAI [4], Ge-PAI [5], and Xe-PAI [3].

FinFET CMOS doping

Both SOI and bulk FinFET structures are doped using high tilt implantation. However, retained dose, one of the concerns with high tilt implantation, is affected by dose loss due to the cosine angle effect at higher tilt angles and sputter or reflection dose limit at lower implant energies and higher doses. Plasma implantation has been studied as an alternative to improve conformal chemical doping, but recent results have shown to be not truly conformal with severe FinFET erosion [6]. However, beam-line molecular dopant implantation up to 60° tilt with Flash MSA was reported to enhance dopant activation [7]. They observed that monomer B at 45° tilt with retained dose >1.1E15/cm^2 had the lowest electrical activation level (B_{ss}=2.8E19/cm^3) when using MSA (**Fig. 5**), while $B_{18}H_{22}$ at a tilt

Thermal processing issues *continued from page 15*

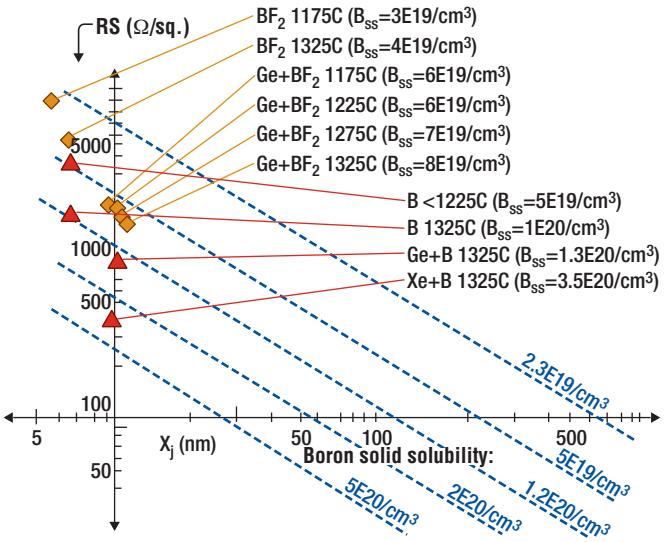

Figure 3. R_s versus X_j chart for monomer B and BF_2 p+ USJ.

of 60° had a retained dose of 5.5E14/cm^2 but the highest dopant electrical activation level (B_{ss}=1.1E20/cm^3). Therefore, conformality and highest electrical dopant activation level are more important for 3D structures when using MSA than the conformal retained chemical dopant level, and the best results were realized using $B_{18}H_{22}$ molecular dopant compared to monomer B and BF_2 [7].

MSA process and equipment design issues

MSA from 1100° to 1350°C enhances USJ dopant activation, especially when PAI or a self-amorphous layer is present as shown in Figs.3 and 5. But these processes do not completely eliminate unstable residual implant damage unless >1300°C, or they are in combination with a low-temperature 900°C spike/RTA annealing step as shown in Fig. 4 (which shows improvement in junction leakage current).

At the 45nm node, most logic and foundry companies introduced either Flash lamp or sub-melt laser MSA in combination with >1020°C spike/RTA in manufacturing. Due to wafer thermal shock, a continuing concern with Flash annealing is wafer slip, warpage, and breakage, requiring special hardware, limited process space, and lots of confidential know-how to avoid it. Wafer breakage can also occur with laser annealing, though not as commonly. However, with laser annealing, localized hot spots (+50°C) can occur [8], causing poly-Si line breakage. The drive to higher MSA peak temperatures for certain benefits and the need for lower MSA peak temperatures for others necessitate a compromise solution that will be different for each customer's confidential implementation.

With Flash lamp MSA, the dwell times are 1–50msec, but if the dwell time is too short, incomplete recrystallization will occur leaving a shallow surface amorphous layer [9]. The number one concern with Flash MSA is wafer breakage caused by thermal shock dependent on substrate type (p/p+ epi wafer, hydrogen denuded HAI-wafer, SOI wafer, etc.) and prior wafer edge damage requiring wafer pre-screening. Increasing Flash pre-heat temperature above 450°C before the MSA step minimizes thermal stresses, but can cause complete recrystallization of the amorphous layer before the MSA step and/or TED (transient enhanced diffusion). Using a hot chuck for pre-heating limits the upper temperature to <650°C, and therefore the peak MSA temperature to <1250°C to avoid wafer breakage. With bottom lamp pre-heating the lower limit is >650°C and peak MSA can be >1350°C before wafer breakage. Flash lamp heating non-uniformities and pattern density effects have been reported to cause ±60°C temperature variation across the wafer [8].

With sub-melt laser MSA, dwell times from 100µsec to 1msec are used and shorter dwell time minimizes localized stress. Wafer warpage/slip due to thermal stresses can lead to lithography overlay problems [10]. Similar to Flash MSA, higher wafer pre-heat temperatures reduce thermal stresses, but 400°C is typical to avoid recrystallization of amorphous layers. With laser MSA the overlap stitching pattern can lead to local non-uniformities [5].

Laser wavelength effects and Brewster angle incidence also influence pattern sensitivity effects, especially with poly and metal lines, requiring some companies to do quad-mode (4× wafer rotation) for uniform annealing around the gate stack structure. Faster cool-down than Flash, due to additional cooling from cold wafer around laser spot, minimizes diffusion but also causes localized thermal stress.

All MSA techniques use three variables for process optimization: peak temperature, pre-heat temperature, and dwell time. Temperature measurement (with patterns) on this sub-msec time scale with feedback for temperature control is very difficult [10]. Cost-of-

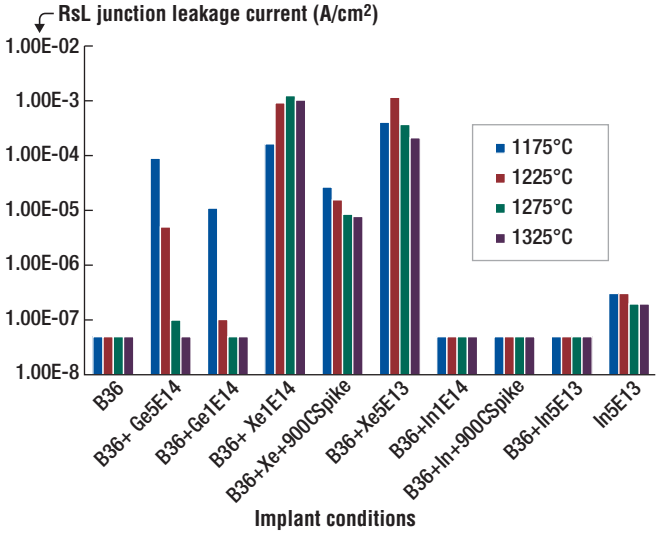

Figure 4. Laser annealing temperature effects on junction leakage current.

ownership (COO) issues include throughput, reliability, and light source lifetime. Integration issues with strain-Si technology and high-*k*/metal gate stack structures are also concerns. With eSiGe strain technology the Ge content can reduce the surface melting temperature by 200°C, limiting the maximum MSA peak temperature to <1200°C to prevent strain relaxation. Reducing the laser anneal dwell time also helps, as does choosing an implant species that minimizes damage/amorphization in the eSiGe region. With eSiC the opposite is observed: for maximum carbon substitutional (C_{sub}) formation, MSA peak temperature must be >1300°C. Failure

continued on page 20

INDUSTRY FORUM

The recession's silver lining: a mandate for more efficiency

Semiconductor industry recessions have given launch to many sub industries over the past 40 years. In fact, if one annotates the birth of the many jettisoned segments on the semiconductor industry compound annual growth rate (CAGR) sinus wave that we have all endured, you can see that the package and test segment emerged in 1972; EDA formed in 1982; and foundry, IP, and design services developed in 1992, reaching escape velocity in 1996. The result has been several, multi-billion-dollar segments with honed value propositions, economies of scale and aggregation, and an increased pace of technological innovation.

The mechanism worked like this: demand sunk, fixed costs had to be reduced, and savvy CEOs instructed their operations folks to find a variable cost solution to deal with the weaker economy. The response during the 1972 recession was to outsource to package and test companies — and a segment was born. Eighteen months later, demand returned and the operations management said to the CEO, "I guess we should rehire all those packaging and test folks and rebuild the lines." Of course the CEO said, "Not so fast. The specialized suppliers that we are using are cheaper and better than us, and they remain a variable cost. No more internal packaging, thank you very much."

The emergence of a commercial EDA industry followed suit, and foundry was not far behind. There were common threads: cost, complexity, and a mandate to focus on one's core value to the markets you service. Today, virtually no company can or should perform any of the functions available from this outsourced ecosystem — and they do not.

There is another outsourced segment coming into its own as this is written: back end operations. Back end operations include the activities from net list or GDS II to end-of-life. "Operations" is the only internal function remaining that has been allowed to exist with gross inefficiency, little to no scale, and technological shortfalls; but not any more.

There is another segment now following the outsource trend: back end operations.

The recession of 2008 has now caused CEOs to revisit the fixed cost issue and examine the sub-optimal operations contribution. The result is that they are calling upon value chain producers to provide a variable and lower cost solution with aggregated expertise and scalable learning. In short, internal operations are on their way out the same way EDA began to disappear as an internal function in 1982.

Jack Harding, *eSilicon Corporation, Sunnyvale, CA USA*

Of course, many larger fabless companies will respond with the equivalent of the now infamous, "Real men own fabs." But we all know what happened to them — it just took a little longer. In the meantime, other than the very largest semiconductor firms, the majority of companies doing any kind of chip design will transition from expensive internal ops teams to an outsourced aggregated operations model.

The result of this recession-motivated change in the semiconductor industry will be efficiency, technological advancement, and a refocus of precious resources onto innovation and product development — where they belong.

No one likes a recession. But if a byproduct of this one is a purge of waste and a reordering of the ops function, well, it can't be all bad. ■

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Harding wrote on the subject of horizontal specialization during a down economy in *The specialization imperative,* co-authored by Mark Templeton. Read this archived article online at www.solid-state.com.

Advanced Packaging

WAFER BONDING

Pressure indicating film characterization of wafer-to-wafer bonding

EXECUTIVE OVERVIEW Wafers are bonded by applying precise combinations of physical pressure, temperature, and/or voltage. Pressure is measured as an average, assuming perfectly flat pressure plates. Applied pressure characterization is important for high yielding eutectic/thermocompression bonds.

Wafer-to-wafer bonding has become an enabling semiconductor technology in industries such as 3D packaging, MEMS, MOEMS, and SOI. In a typical wafer bonding process, two flat substrates are permanently joined (bonded) to one another by applying precise combinations of physical pressure, temperature, and/or voltage (**Figure 1**). Each of the above factors is set depending on the substrate materials being bonded, and the control of these parameters is crucial to a successful, high-quality, high-uniformity manufacturing process.

Of these major parameters in a bond recipe, voltage and temperature are readily measurable within a wafer bonding chamber using common electronics and thermocouples. Pressure, on the other hand, is measured in the tool as the total amount of force exerted over the pressure column. This measured force is then used to calculate the average pressure, assuming perfectly flat pressure plates. In practice, the pressure plates are often non-ideal, or they may have degraded over time. This leads to potential pressure variations which would not be detected with control software alone. Such poor distribution of pressure can lead to unbonded wafer areas, cracked wafers, or even premature wear of the pressure plates.

The significance of a uniform applied pressure in a bonding process depends largely on the specific materials being bonded. For example, in an anodic bonding process, silicon is bonded to glass (typically Pyrex) by applying a large electric field (e.g. 1000V) at elevated temperatures (e.g., >300°C). At such temperatures, sodium impurities in the bulk of the normally insulating glass becomes mobile, thus making the glass much more conductive. When a high voltage is applied to the anode in this state, the sodium ions move toward the anode, leaving oxygen ions at the bond interface. The reaction between silicon and oxygen forms a strong SiO_2 bond.

The applied voltage also creates a large electrostatic force on the bond stack, which assists with the bonding process. Because the magnitude of the electrostatic pressure is generally sufficient for a full bond, physically applied pressure is neither critical nor required for this type of bond process.

However, in an eutectic/thermocompression bonding process, two arbitrary substrates are bonded together using thin intermediate films that are often metallic alloys (Fig. 1). A common bond metal for silicon is Au-Si eutectic bond with a eutectic temperature of 363°C. In this bond, the Si surface contacts Au deposited on the other substrate, and the stack is brought to a temperature just beyond the eutectic point for a short time to allow the alloy to form. Given a fixed temperature, if too much pressure is applied, the eutectic alloy can spill out into unwanted regions and cause short circuits. Conversely, too little pressure would typically result in weakly bonded or unbonded regions. And in practice, spill outs and unbonded regions are often found on the same pair of substrates due to pressure and/or temperature non-uniformities. Therefore, the characterization of applied pressure is important for these bond processes to achieve high yields.

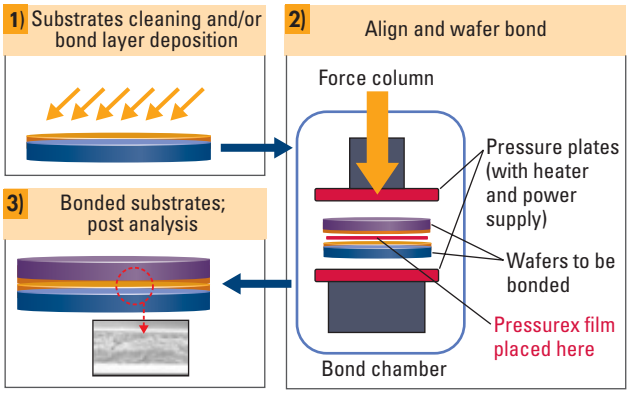

Figure 1. Wafer bonding process.

Pressurex film (Sensor Products) is a direct and economical way to detect and correct such pressure variations. The thin flexible film measures pressure from 2–43,200 PSI (0.14–3,000 kg/cm^2). When placed between contacting surfaces of a wafer bonding fixture it instantly and permanently changes color directly proportional to the amount of pressure applied. The precise pressure magnitude is determined by comparing color variation results to a color correlation chart (much like interpreting Litmus paper).

By running a bond recipe with the pressure set to 4 bar on an appropriate grade of pressure film, a direct imprint is

Kwan-yu Lai, Micralyne, and **Jeffrey G. Stark**, Sensor Products

formed. **Figure 3** shows Pressurex Micro sensor film 2–20 PSI (0.14–1.4 kg/cm^2) taken from a 6" diameter bonding tool with poor pressure uniformity. Analyzing the pressure distribution with the Topaq Tactile Force Analysis System, this image is transformed into a color-coded pressure map, revealing a high-pressure ring (>10 bar) with relatively little pressure applied at the center. The line scan further elaborates these pressure inconsistencies.

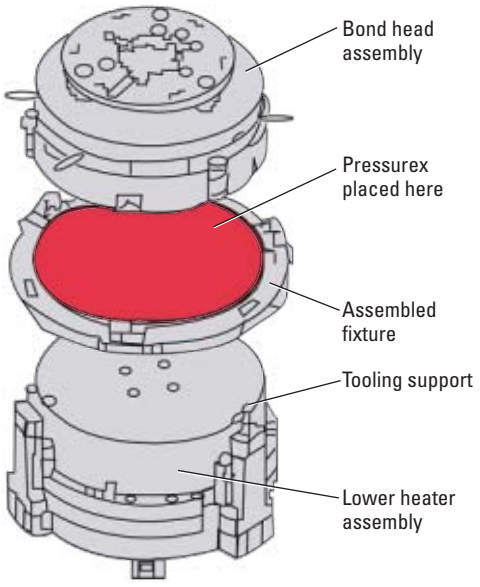

Figure 2. Magnified image of a wafer bonding fixture shown with pressure sensor film in place.

A series of adjustments to the pressure column of the bond tool were made, and the pressure uniformity was checked each time by running the same bond recipe on the same range of pressure film. The resulting series of images are shown in **Figure 4**, which confirms that the actual pressure is more uniform. After the adjustments, the pressure film analysis shows an offset from the intended recipe pressure of 4. By using properly calibrated pressure film, the offset can be corrected. Similarly, it can also be used to match processes across multiple bond tools.

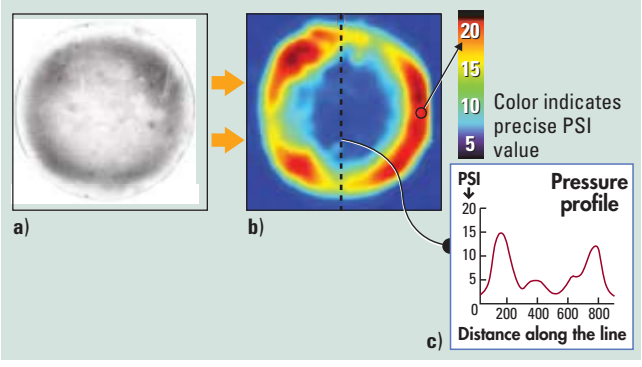

Figure 3. Bond tool images show pressure inconsistencies.

The same pressure film can be used as a tool performance log in manufacturing practices such as Six-Sigma statistical process monitoring. Cost savings will inure to users of pressure indicating film through decreased scrap rate and increased time efficiency. There are also specific benefits that are distinct to each type of bonding application.

Metal eutectic bonding

Pressure film prevents the eutectic alloy from spilling out into unwanted regions and causing short circuits, which, given a fixed temperature, can occur if too much pressure is applied. It also can minimize weak bonded or un-bonded regions that occur if too little pressure is applied. Pressure film reveals the magnitude and distribution of pressure across the bonding platen and part.

Anodic bonding

Here, the film reveals whether the top and bottom plates are in uniform contact.

Fusion bonding

The pressure film can help minimize trapped air pockets between the bonded substrates, which on certain applications can be caused by non-uniform applied pressure.

Metal diffusion bonding

Using the film can help minimize un-bonded wafer sections, detecting if pressure is too low. Wafers won't bond if the forces are too low.

Glass frit bonding

Pressure indications can ensure hermetic seal is formed around the device, which will not occur if pressure is too low. Overly high pressure could prevent the glass frit from flowing into the device.

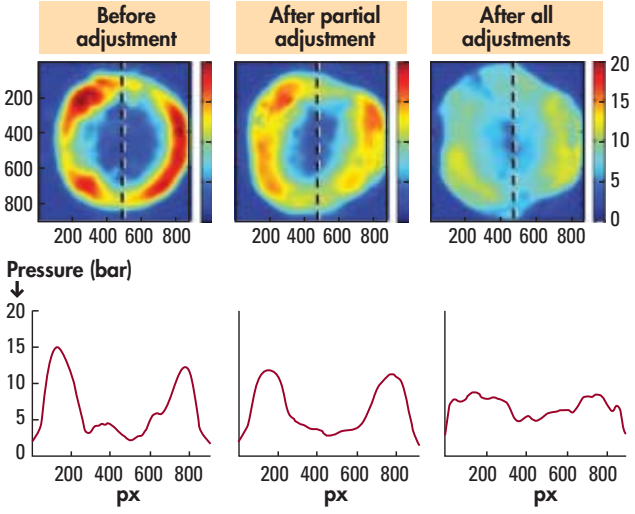

Figure 4. Bond tool images show improvement to the pressure uniformity as captured by pressure-indicating film.

Polymer adhesive bonding

Use pressure measurement to minimize voids caused by polymer thickness non-uniformity. While this is not a direct problem related to the amount of pressure, pressure non-uniformity can exacerbate the problem.

Conclusion

Pressure-indicating film is a quick and direct research tool that provides a snapshot of the pressure distribution of a bond tool at room temperature. Through calibrated post analysis, it also

Wafer-to-wafer bonding *continued from page 19*

provides a method to compare processes and tools implemented during manufacturing. ■

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Thermal processing issues *continued from page 16*

of high-*k*/metal gate structures at >1300°C MSA temperatures must be avoided [11].

Conclusion

Scaling CMOS junctions for the 22nm node requires a combination of ultra-low energy beam-line dopant implantation down to 83eV dependent on the surface oxide thickness; self-amorphization or optimized amorphization of the near-surface silicon region, to maximize dopant activation with diffusion-less annealing; and defect stabilization to reduce junction leakage and residual implant damage with diffusion-less msec annealing only, or in combination with a low temperature (<900°C) spike/RTA annealing. These junction scaling techniques can be applied to planar and FinFET CMOS device structures. However, high-temperature msec annealing using Flash lamp or sub-melt laser annealing equipment can cause catastrophic device and wafer yield loss if not carefully optimized. ■

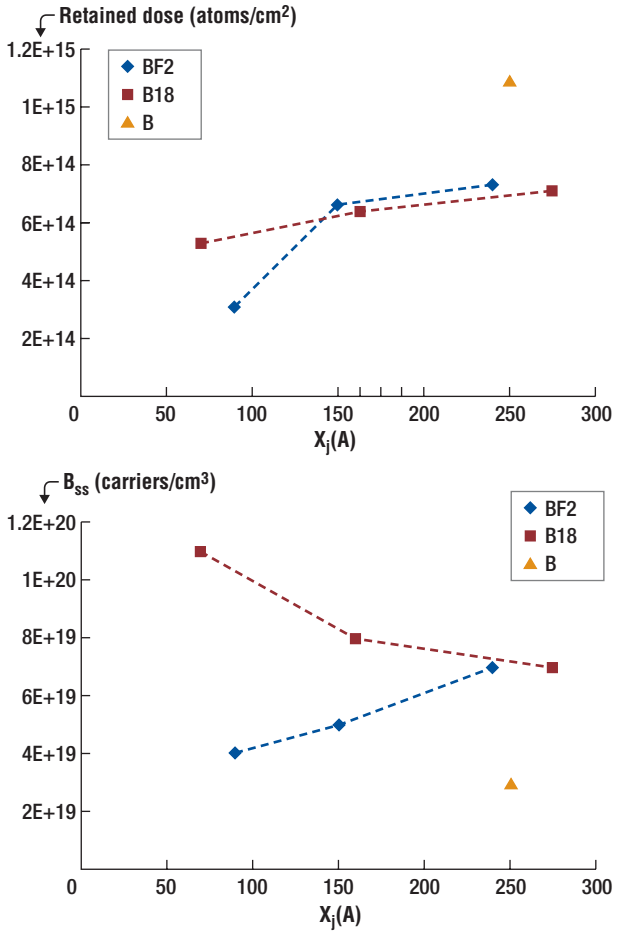

Figure 5. Effects of X_j at 60° tilt angle for BF_2 and $B_{18}H_{22}$ and 45° for B on a) PCOR-SIMS retained dose and b) B_{ss} dopant activation level.

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DEFECT DETECTION

Non-visual defect inspection for comprehensive yield management

EXECUTIVE OVERVIEW As new materials, processes, and structures are introduced at sub45nm nodes, surface quality requirements are becoming more stringent. Surface quality control issues can give rise to organic and metallic residues, charging, and other non-visual defects (NVDs). Whereas yield management strategies previously focused solely on physical defects such as particles and scratches, NVD inspection is becoming an integral part of yield management at these nodes.

NVDs are defects that do not have measurable physical dimensions in the traditional sense. While they can cover large areas of a wafer's surface, they are often sub-monolayer or electrical in nature, having the Z-height of a single atom or molecule. NVDs cause changes to the electrical or chemical properties of the wafer surface that can lead to poor adhesion of subsequent layers, degraded device parametrics or long-term reliability issues. The International Technology Roadmap for Semiconductors (ITRS) cites the increasing importance of NVDs for yield, and the need for new NVD inspection techniques at advanced design nodes [1].

Many NVDs result from suboptimal cleaning and surface preparation due to the liquid-contact nature of the step. These NVDs can come from the wafer, the liquid, the interaction between liquid and wafer, or the environment. NVDs include:

Organic contamination. For example, new resist formulations or etch processes may result in incomplete resist stripping when cleaned using an existing process of record.

Metallic contamination. For example, copper (Cu) contamination of a bath can cause subsequent cross-contamination of wafers exposed to that bath.

Process-induced charge. Charge can buildup on the wafer's surface during the final rinse, especially on insulators cleaned in single-wafer tools.

Carrier-induced outgassing. Plastic containers such as FOUPs and FOSBs can outgas compounds that react with residual wafer cleaning solvents to form insoluble organic salts at locations close to the carrier touch points.

Airborne/surface molecular contamination. Adsorption of AMCs during wafer queuing can lead to surface molecular contamination, which may be the AMC species or a compound formed by the AMC species and the material on the wafer surface.

NVD defect detection is quite different than for physical defects, such as particles. Because of their relatively large height, physical defects scatter incident light. They are typically detected using optical inspection techniques, such as brightfield and darkfield imaging or laser scatterometry. NVD Z-height is too small to scatter light, precluding optical detection.

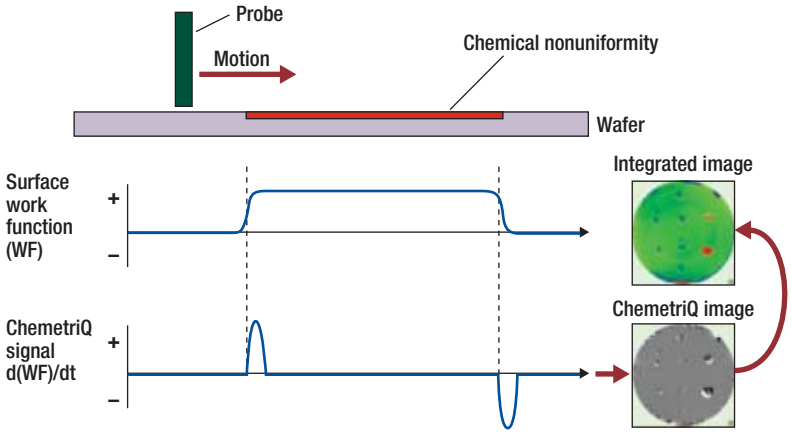

Figure 1. The SPDI method uses work function sensing to detect NVDs on the wafer surface.

I review a new NVD inspection technique, describing several case studies of NVD issues impacting yield, and explore the economics of NVD inspection.

Incorporating NVD inspection into yield management

Because optical inspection techniques cannot detect NVDs, other means are needed. One such technology is the ChemetriQ system, which uses surface potential difference imaging (SPDI) to detect changes in the work function and charge of materials [2].

The SPDI method spins the wafer and holds a probe close to (but not contacting) the wafer surface (**Fig. 1**). Where the surface is completely uniform, a constant voltage results that is proportional to the difference in work functions of the probe and the wafer. When a non-uniformity is encountered, the change in work function causes a change in voltage on the probe tip, which is proportional to the rate of change in work function on the wafer, d(WF)/dt. This change

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Non-visual defect inspection continued from page 21

is detected and mapped over the entire surface of the wafer to form the ChemetriQ image in Fig.1. A simple mathematical integration then produces the integrated image that shows regions of NVDs on the wafer.

With the increasing impact NVDs have on device yield, yield management strategies must incorporate NVD inspection and review in a way that is analogous to physical defect inspection — both in-line to prevent excursions that can affect line yield, and in the lab to assist with root cause analysis and process development. Inspection can help pinpoint NVDs in production. These locations can then be exported to analytical tools such as TXRF or TOF-SIMS, which provide detailed summaries of NVD materials.

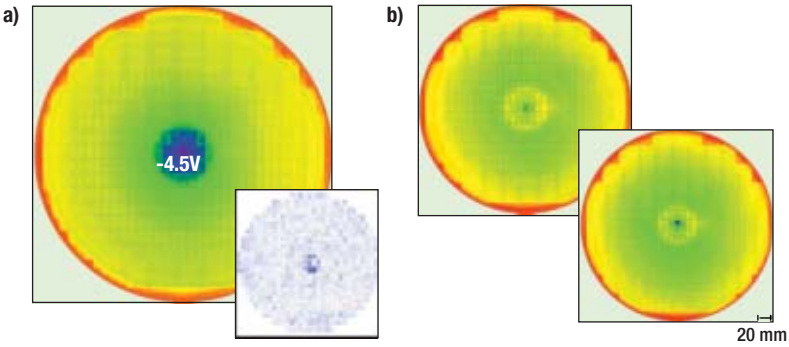

Figure 2. End-of-line yield maps correlated to a charging signature from a single wafer clean tool a) that was significantly different from other tools b).

In the following examples of NVDs impacting device yields, practical implementation of NVD inspection isolated their source and eliminated the NVDs.

Process-induced charging in a 45nm logic fab

Process-induced charging is a growing source of yield loss. New materials, thinner film stacks, and smaller geometries are more easily damaged by charge. New techniques such as single wafer cleaning can introduce new sources of process-induced charge into the process. Because charging cannot be detected by optical inspection, traditional yield management tools are "blind" to this issue.

A major logic manufacturer recently experienced a charge-related yield issue on its 45nm line [3]. End-of-line yield maps (**Fig. 2a**) showed that center dice covering ~2% of the wafer were consistently non-yielding. Further analysis via tool commonality studies pinpointed the probable source to a specific chamber on a single wafer cleans tool. However, none of the existing inspectors in the production line were able to capture a defect pattern matching this center of wafer signature, making it impossible to isolate the source and eliminate the root cause of the yield loss.

SPDI inspection, however, highlighted a center of wafer charge gradient, whereby the outer regions of the wafer exhibited a -1.5V charge level compared to -4.5V for the center area. Comparisons were done to other chambers running the same cleans process, which showed much lower levels of center-of-wafer charge (Fig. 2b). The process engineers designed and performed a number of experimental splits to better understand the nature of the charge signatures, and to assess how tool and process parameters contributed. The experimental results indicated that the charge levels could be optimized with a tool configuration using a shield plate, N_2 ambient purge, and a 60sec. dilute HF etch time.

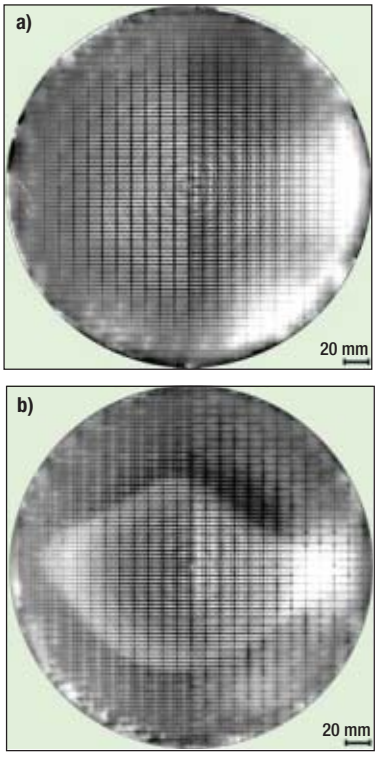

Figure 3. A reference DRAM back end of line wafer a) and a wafer with poor resist strip b).

Organic contamination in a 32nm DRAM fab

Innovative resist formulations are in development for advanced design rules. In the front end, more complex structures, double-patterning, and immersion lithography are driving these new formulations. In the back end, new integration and interconnect schemes also encourage new lithographic techniques with new resist requirements. A critical issue in using new resists is that if they are not completely stripped from the surface after etch, organic NVDs can cause subsequent adhesion and reliability issues.

At a major DRAM fab, SPDI inspection was used to evaluate resist strip efficacy [4]. **Figures 3a** and 3b show two back-end wafers, one reference, the other after a poor resist strip step. The large signature in Fig. 3b

	Memory	Logic
Model Inputs: Fab Economics		
Wafer starts per month – ramp start	20,000	10,000
Wafer starts per month – full production	60,000	40,000
Baseline time: 25% to 90% yield (months)	24	24
Devices / 300mm wafer	1480	200
Starting ASP / die	$2	$20
ASP fall rate per month	3%	3%
Model Inputs: NVD Ramp Yield Improvement		
Average # dice per affected wafer per event	8	4
% of wafers affected by each event	100%	8%
# of events during ramp	6	6
Model Inputs: NVD Production Yield Improvement		
Events per year per wet clean bench	2	2
Model Results:		
Peak Improved Yield During Ramp	3.20%	0.90%
Long Term Production Yield Improvement	0.54%	0.54%
Peak Monthly ROI	$1.2m	$0.6m
Cumulative ROI – 2 Years	$19.5m	$8.8m
Cumulative ROI – 5 Years	$25.5m	$20.4m

Table 1. Inputs and results of the model show a significant return on investment (ROI) for NVD inspection.

shows the organic residue pattern from the incomplete resist strip. The wafers also exhibited different SPDI signatures on the left and right halves due to the presence of Al contamination from open fuses on the left half of the wafers.

New process flows at this fab historically required many specific surface analyses such as ToF-SIMS and AES to optimize resist strip and cleaning sequences. With the SPDI inspection's ability to perform fast scans of experimental wafers, with visual indication of residue locations, the number of analytical scans is greatly reduced and learning cycles accelerated.

Economics of NVD inspection

The previous examples highlight how NVD inspection was able to provide insight to yield issues that traditional optical inspection approaches could not, shaving weeks or months from the time to identify and solve yield problems. This enables a faster yield ramp, allowing a fab to capitalize on the "sweet spot" in device pricing — the higher average selling prices (ASPs) that accrue to advanced devices in the early months of their manufacture [5]. These economics can be modeled as shown in **Table 1**. Begin with typical fab economics such as wafer starts, die size, ASP trends, and typical yield ramps; for example, a state-of-the-art 25–90% ramp in 2 years. Model ramp yield events (events that are caught and solved sooner via NVD inspection), with an average percentage of dice and wafers affected per event. For example, in one DRAM fab an average of 8 dice/affected wafer, on 100% of wafers, were found at 6 steps, whereas the logic charging example described above affected 4 dice/wafer on 1 out of 12 cleans tools, or 8% of wafers affected. Model production events by estimating frequency and impact of NVD events that occur annually per cleans tool.

Figure 4 shows how these values play out over time for the DRAM example. The upper chart shows that the yield at a given point during the ramp is as much as 3.2% higher with NVD inspection. With the relatively high ASPs at that time, fab profitability benefits dramatically — peaking at over $1.2m per month, as shown in the lower chart. Benefits continue into the production phase, as NVD-related yield excursions are prevented. Cumulatively, the result is a 5-year return on investment (ROI) of $25.5m. The trends for the logic case are similar, with the values shown in Table 1. ■

Conclusion

The arrival of new semiconductor device structures and processes are giving rise to NVDs, which require new ways of thinking about yield

Non-visual defect inspection continued from page 23

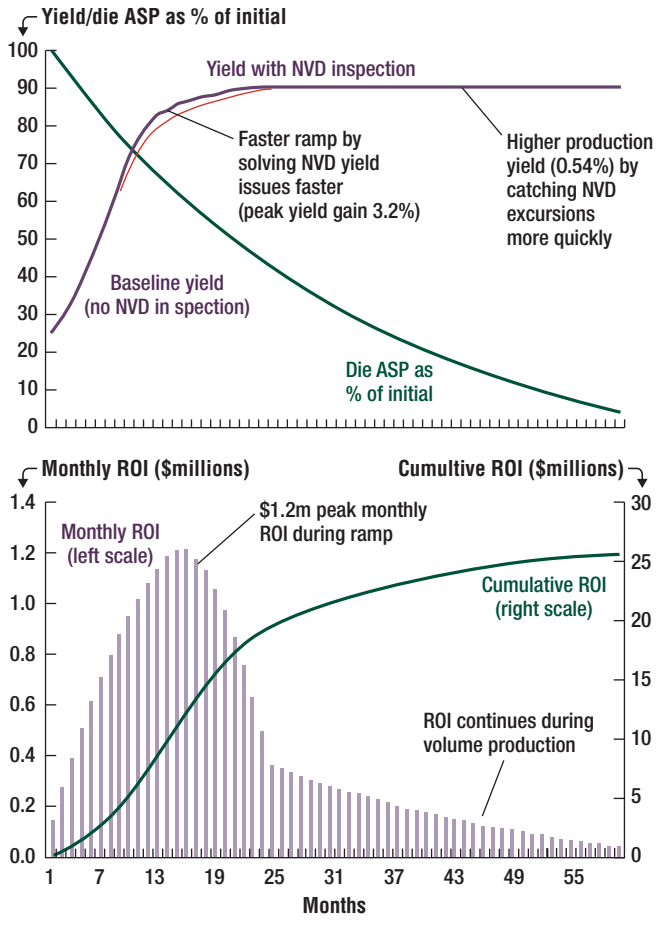

Figure 4. Modeled 5-year ROI for implementing NVD inspection in a DRAM fab.

management. Incorporating inline NVD inspection into a yield management strategy can have a compelling ROI for the fab.

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Paula Mints
Principle Analyst PV
Services Program
Navigant Consulting

James Gee
Founder, Chief Scientist
Advent Solar

This Webcast explored these recent advances through presentations from some of the industry's most innovative companies. The presenters shared their insights and discussed the challenges ahead in photovoltaic solar cell design and process development. The discussion segment handled the issues of the day. Attendees were able to apply what they learned to maintain their company's competitive edge.

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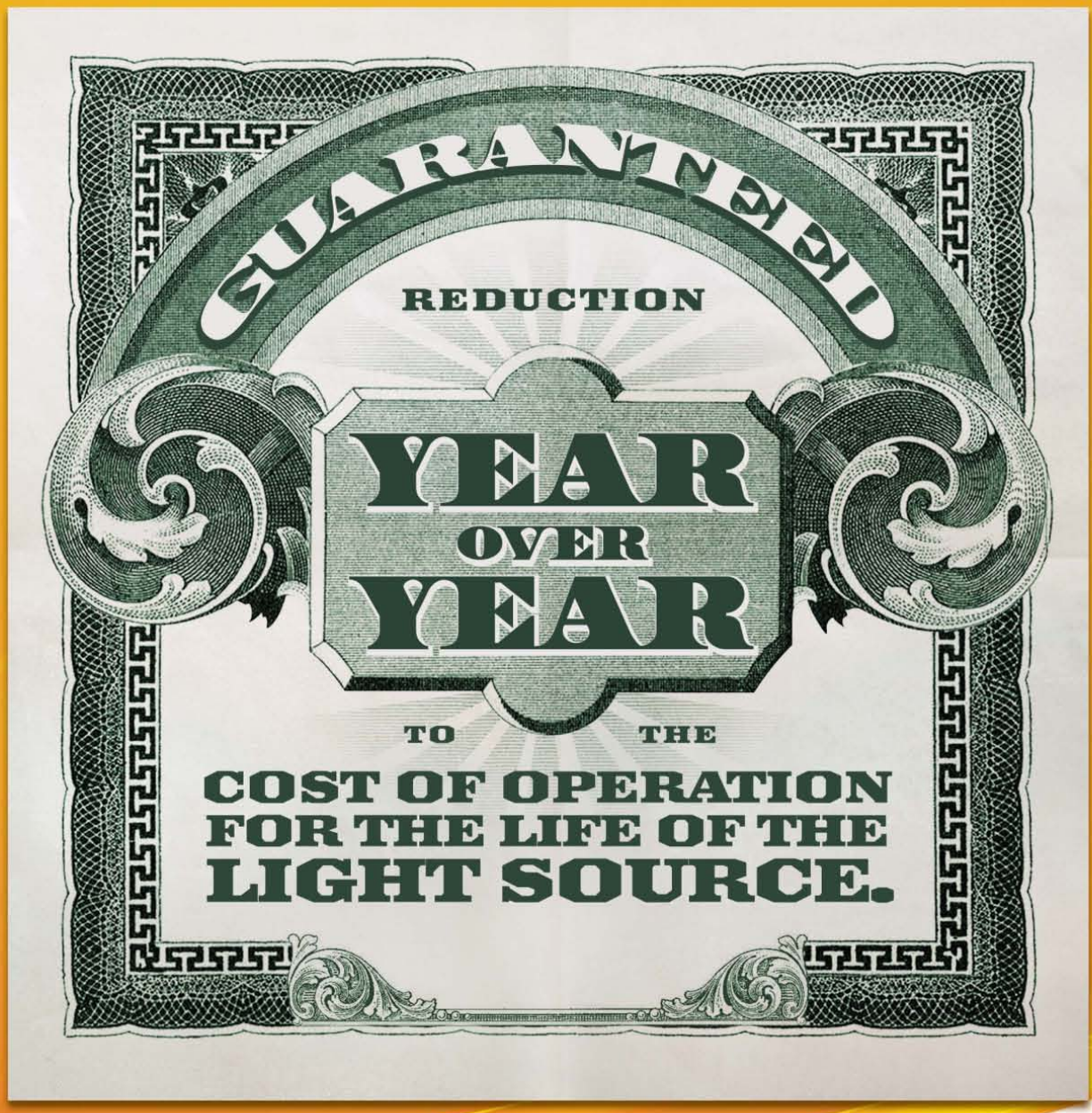

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