Implant And Annealing Process Integration Issues To Reduce Device Variability For <10nm p+ & n+ Ultra-Shallow junctions

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Abstract

Both p+ and n+ ultra-shallow junctions (USJ) <10nm deep have been realized by using <200eV equivalent boron energy (<890eV BF2 or <4keV B18H22) or <1keV equivalent arsenic energy (<500eV P or <1.7keV Sb) implants in combination with diffusion-less high temperature msec annealing and diffusion-less low temperature spike annealing thereby also reducing device micro-variation. Non-contact optical metrology techniques such as therma-probe (TW) and junction photo-voltage (RsL) were used to detect and monitor both implant and annealing equipment micro-uniformity and unique equipment signatures as well as junction "quality" (dopant activation, residual implant damage and junction leakage current).

1.Introduction

Sub-10nm USJ will be required for manufacturing in the 2009 to 2012 time frame. Such shallow junctions can be realized using deep pre-amorphous implant (PAI) layers such as Ge but after dopant activation annealing the residual implant damage/defects caused by the amorphous layer leads to end-of-range (EOR) defects beyond the junction and junction leakage degradation therefore poor quality junctions as shown in Figs. 1 & 2 [1,2,3]. If the EOR damage was located within the junction then good junction leakage current was realized but as the damage approaches the junction the leakage current increased by orders of magnitude and saturates as it goes beyond the junction. This effect is shown in Fig.2 for different diode junction leakage current measurements with SPE annealing [1,2,3]. Therefore, monitoring junction leakage current is an important USJ parameter for determining junction quality.

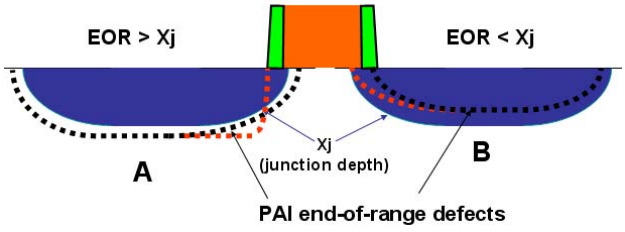

Fig.1: Location of EOR damage on junction quality [1].

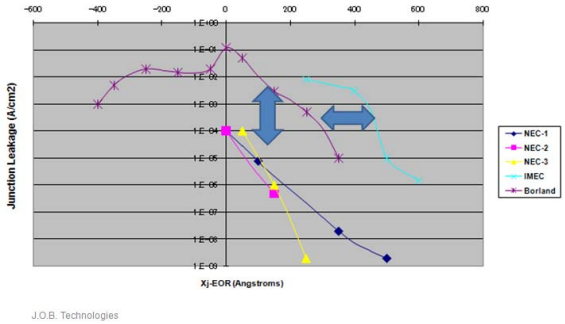

Fig.2: Different diode junction leakage current results for various PAI EOR damage depths [1,2,3].

2.USJ Implantation

To realize implant junction depth <10nm before diffusion, p+ extension will require monomer boron implant energies 150-350eV without channeling as shown in Fig.3 while n+ extension using arsenic implant would be <1.5keV, Phosphorus implant <1keV and Antimony implant <2keV [4]. With near zero dopant diffusion in the vertical and lateral direction under the gate, the angle and dose precision/control of the extension implant becomes very critical to reduce device variation both within a wafer and wafer to wafer. Kuroi of Renesas reported that variation in local implant angle resulted in asymmetrical transistor as well as Vt (threshold voltage), Lg (gate length) and gate delay degradation [5]. Therefore the implanter equipment design can have a direct impact on device variation with diffusion-less dopant activation techniques [6,7].

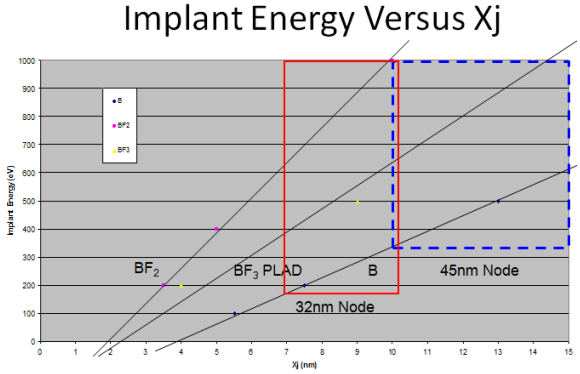

Fig.3: Boron extension implant energies without dopant channeling [4].

There are 2 basic equipment designs for single wafer high current implanters, either ribbon beam or spot beam and they each have a unique non-uniformity signature based on angle and dose precision [8]. Fig.4 shows therma-probe detection of implant micro-variation for a ribbon beam implanter [9]. Any localized implant variation for a zero tilt extension implant can be reduced by using quad-mode wafer rotation implantation. Alternatively, changing dopant species can also reduce implant angle sensitivity especially for n-type dopant as shown in Figs. 5&6 were zero tilt lateral straggle under the gate stack edge for arsenic is near zero while for phosphorus lateral straggle is >40% and therefore not sensitive to any implant angle variation [10]. To achieve the desired gate overlap with arsenic would require tilted quad mode extension implantation by up to 30 degrees as shown in Fig. 7 [11]. For spot beam, beam blow-up/divergence effects require changing the p-type dopant species from monomer boron to B18H22 and n-type dopant species from As to As4 or Sb. This will also reduce pattern density dose loss effects due to implantation into the gate stack sidewall as the gate stack to gate stack spacing decreases. Today the choices for implanters include the Varian VIISta-HCS, the Axcelis Optima-HD and HD-Imax (B18H22 ion source), the SEN-SHX and the AIBT i-Pulsar. Another concern is

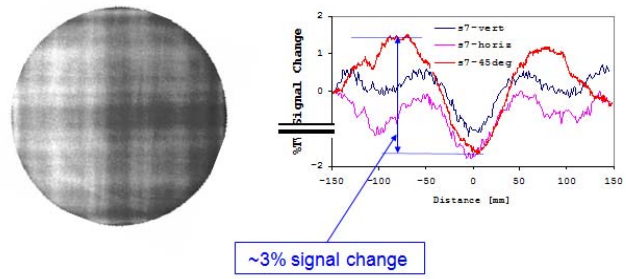

Fig.4: Therma-probe micro-implant variation [9].

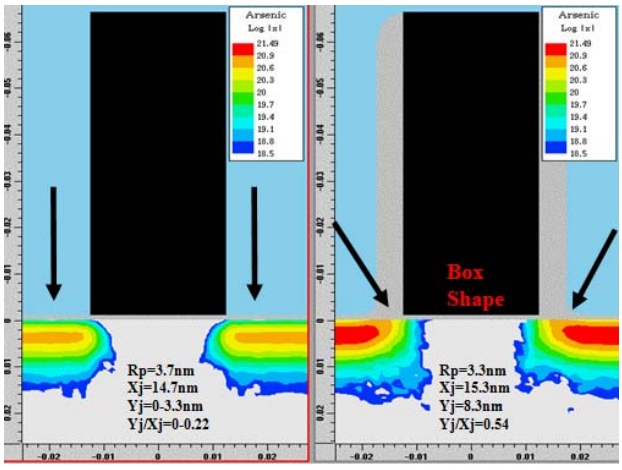

Fig.5: Arsenic 0 and 30 degree tilt implant showing little lateral straggle [10].

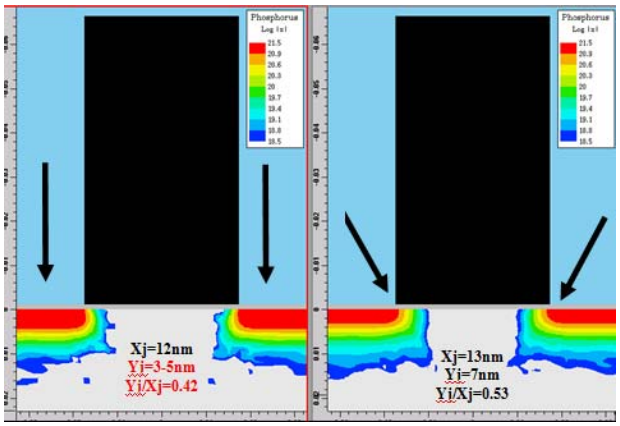

Fig.6: Phosphorus 0 and 30 degree tilt implant showing significant lateral straggle.

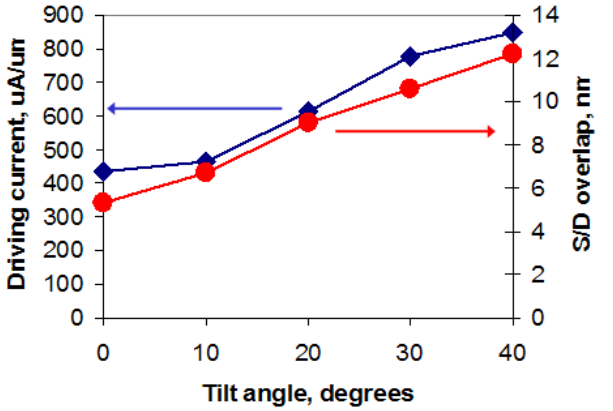

Fig.7: Arsenic tilted extension implantation for improved gate overlap control [11].

energy contamination when running the implanter with large deceleration energies to achieve low energy implants with high beam currents. In the 200eV energy range to keep the energy contamination level below 0.1% usually requires <2.5 to 1 decel ratios though unique beam line designs using energy contamination filtering have reported to allow higher decel ratios >10 to 1.

3.USJ Annealing

The most critical process step to realize high quality USJ is the anneal for dopant activation and implant damage recovery. Current state of the art device manufacturing uses diffusion spike/RTA annealing >1000°C in combination with diffusion-less msec Flash lamp or sub-melt laser annealing in the 1200°C to 1300°C temperature range. This results in 10-20nm of dopant diffusion and is usually done with one of the following 3 different sequences: 1) spike+msec, 2) msec+spike or 3) msec+spike+msec annealing. The best dopant activation is achieved with msec only for temperatures >1325°C. For laser or Flash msec annealing temperatures <1300°C an amorphous layer is

needed for maximum dopant activation by either a PAI layer or self-amorphization but EOR damage beyond the junction will lead to junction leakage degradation as shown in Fig. 2. A spike anneal step will further reduce the EOR damage and diffuse the junction beyond the EOR damage thereby improving junction leakage. The spike anneal will also ensure dopant diffusion through the thick poly gate electrode and eliminate the msec annealing equipment micro-variation signature of the Flash lamp or laser overlap stitching pattern [12]. Fig.8 shows that a 1000°C spike anneal dominates any uniformity effects from a msec anneal as detected by therma-probe full wafer imaging [10]. This effect on improved uniformity is also seen with a 900°C spike+Flash or laser anneal. Petersen also reported laser annealing stitching pattern and localized power variation directly results in 6-9% micro-variation in dopant activation as detected by sheet resistance Rs measurement shown in Fig.9 [13].

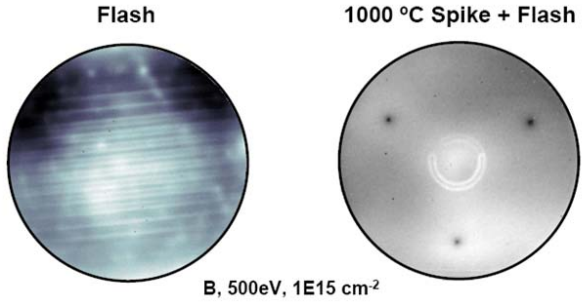

Fig.8: Therma-probe full wafer images comparing Flash only to spike+Flash annealing combination.

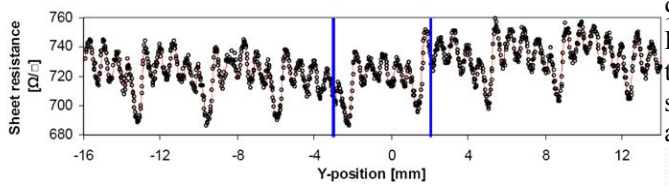

Fig.9: Rs micro-variation caused by laser annealing [13].

4.Process Integration Issues

The best USJ process module may not give the best device performance therefore process integration trade-offs must be considered to optimize these issues. Fig.10 shows how the gate stack structure and process flow can impact the USJ annealing. Selection of strain-Si technology will also impact the USJ annealing options. High temperature will cause eSiGe strain relaxation so lower spike and msec annealing temperatures are required by as much as 100°C to <1200°C for msec annealing. This results in trade-offs between the best USJ dopant activation (Rs), strain-Si relaxation and gate poly activation (Tinv). For example, with doped poly gate electrodes, spike first and msec last annealing gives the lowest poly resistance and best gate oxide Tinv values but worse extension resistance as shown in Fig. 11 [14]. Flow A is for msec+spike and flow B is for spike+msec.

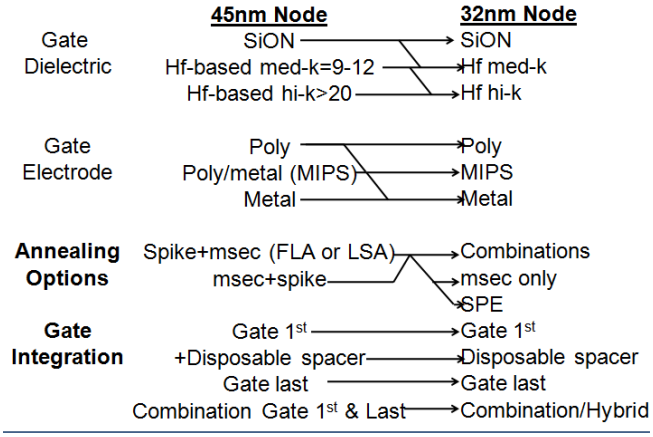

Fig.10: Gate stack integration options.

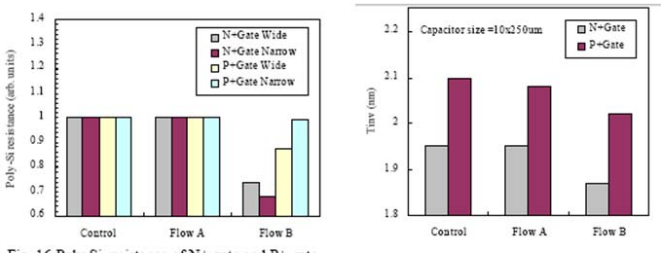

Fig.11: Comparison of gate poly for msec+spike (flow A) or spike+msec (flow B) [14].

If the spike/RTA temperature is reduced to 900°C boron dopant diffusion is eliminated as shown in Fig.12 [15]. Appling this low temperature spike anneal to msec annealing also eliminates the Flash and laser stitching pattern, reduces amorphous layer EOR damage and retains the msec dopant activation benefits [12].

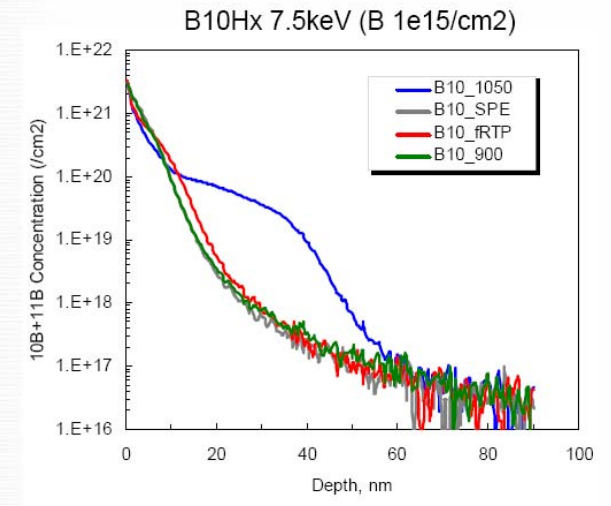

Fig.12: Diffusion-less spike annealing at 900°C [15].

The 3 main areas for device leakage degradation are 1) gate leakage, 2) source drain junction leakage and 3) gate edge junction leakage at the extension and HALO due to band to band tunneling. These areas can be seen in Fig.13. Switching to high-k/metal gate stack structure will reduce the gate leakage by 100 to 1,000 times compared to SiON/poly gate stack. Engineering the location of the residual implant damage and EOR damage can reduce source drain junction leakage as shown in Fig.2. But the gate edge junction leakage is more difficult to engineer and influenced by many more parameters including HALO dose and extension abruptness resulting in orders of magnitude junction leakage current variation. Fig.14 shows the effects of HALO dose up to 4E13/cm2, annealing methods (spike, SPE and msec) and also PAI (Ge or Si) on junction leakage current. Additional effects such as changing the Flash intermediate and peak temperatures are shown in Fig.15. Therefore, the optimum annealing conditions for best USJ sheet resistance Rs can be misleading and not result in the highest quality junction when you consider junction leakage current also.

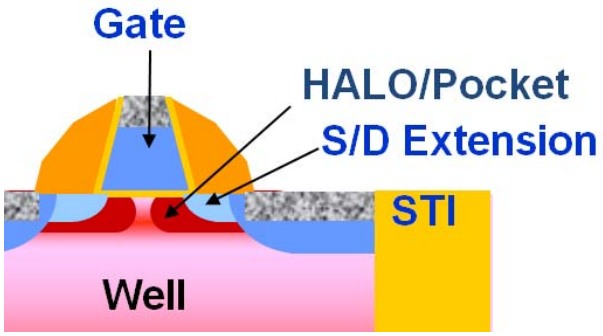

Fig.13: Gate leakage, S/D leakage or SDE/HALO gate edge leakage (band to band tunneling).

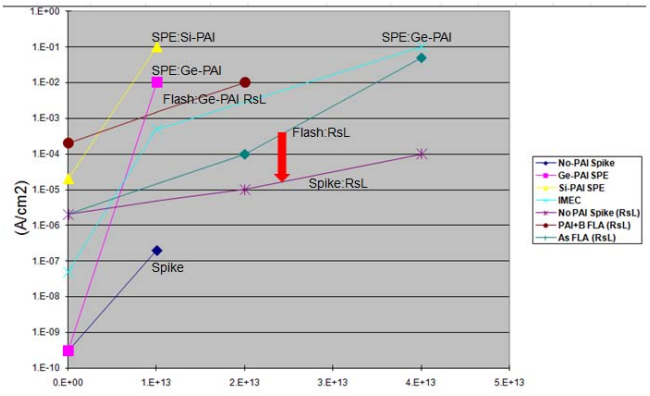

Fig.14: Effects of HALO dose on SDE/HALO leakage.

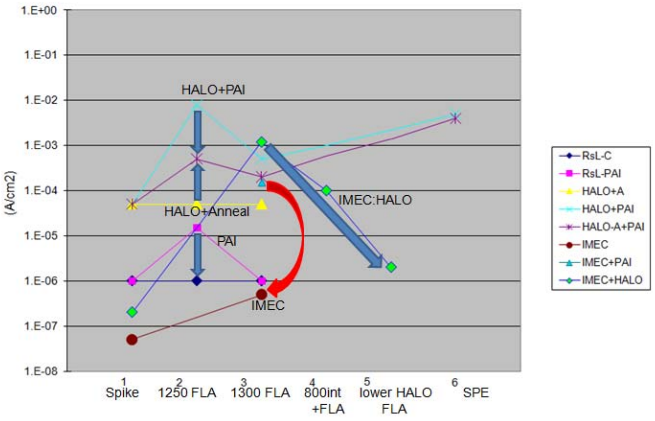

Fig.15: Effects of annealing on junction leakage.

5.FinFET Doping

Logic devices will stay with planar single gate CMOS transistors for several more generations but SRAM and DRAM devices may switch to multi-gate transistor design in the next 1 to 2 generations requiring 3-D doping techniques. Conformal doping of multi-gate 3-D structures will be difficult but there are 3 techniques available: 1) plasma implant doping, 2) CVD deposition doping or 3) high tilt beamline implantation. A few years ago plasma implantation for conformal doping was studied and showed that it was not conformal and there was also a severe sputter dose limit issue as shown in Fig. 16 for BF3 and B2H6. Boron doped CVD deposition has been used in the eSiGe strain-Si technology for deep S/D by Intel since the 90nm node and by AMD for the shallow extension replacing the boron implantation doping step. Next eSiC for nMOS is planned at the 32nm node using deposition and the n-type dopant can also be doped in-situ or implanted separately. The third alternative using high tilt beamline implantation was reported by Duffy of NXP [16]. At high tilt angles retained dose is also an issue as shown in Fig. 17 so B18H22 and As4 may be best alternative dopant species but key is not to completely amorphize the Fin structure.

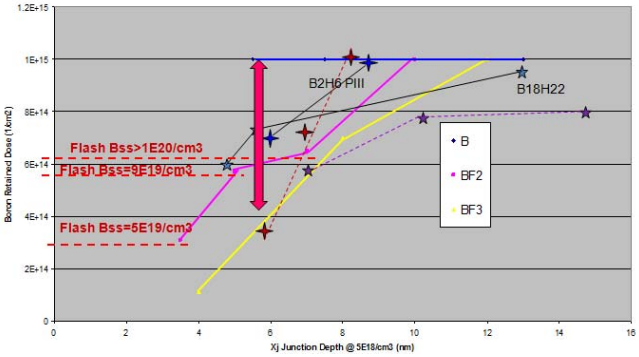

Fig.16: Boron sputtered retained dose limits [4].

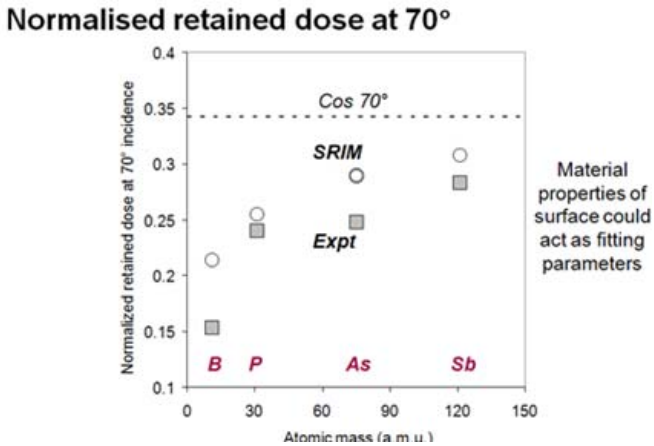

Fig.17: Retained dose versus atomic mass [16].

6.Summary

USJ <10nm deep can be realized with diffusion-less dopant annealing techniques. The combination of diffusion-less msec and 900°C spike anneal is required to eliminate both implant and annealing micro non-uniformities. Switching to B18H22 for p+ and Sb for n+ extension implants also reduces device variation by reducing beam blow-up for spot beam implantation and therefore pattern density dose lose effects. Switching from arsenic to phosphorus n+ extension increases lateral straggle thereby reducing implant angle sensitivity effects and asymmetric transistor with ribbon beam implantation. Therma-wave can detect both implant and annealing micro-uniformity variations with full wafer image mapping while RsL can determine USJ junction quality (dopant activation Rs and junction leakage current).

8.References

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