Monitoring Ion Implantation and Annealing Precision to Reduce Device Variability

John Borland, J.O.B. Technologies, Aiea, Hawaii; Wade Krull, SemEquip, North Billercia, Mass.; Masaharu Tanjo, Nissin Ion Equipment, Kyoto, Japan; Mark Namaroff, Axcelis Technologies, Beverly, Mass.; Andrzej Buczkowski, Nanometrics, Bend, Ore. –

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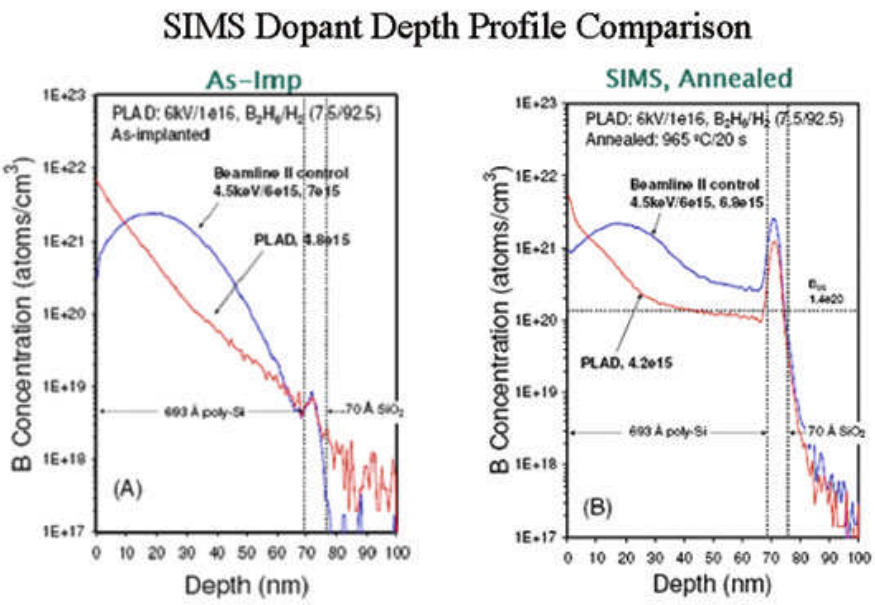
The number of implant steps is increasing with each device generation; for example, with system-on-a-chip (SoC) devices, this can average ~38 implant steps for low- and high-voltage transistors. Implant micro and macro dopant precision and variation directly affect device threshold voltage (V_t) variability for high-energy (HE) and high-current (HC) implantation.[1-4] Therefore, detection and monitoring of any variation in the precision of implanted dopant is critical to reduce device V_t variation as devices are scaled to the 45 and 32 nm nodes.

High current
HC implanters are the largest implant market segment, averaging >51% of the total implant market for the past three years, and greatest implant strategic-added value to device processing. Over the next two years, HC implanter designs must change to address two distinct device requirements:

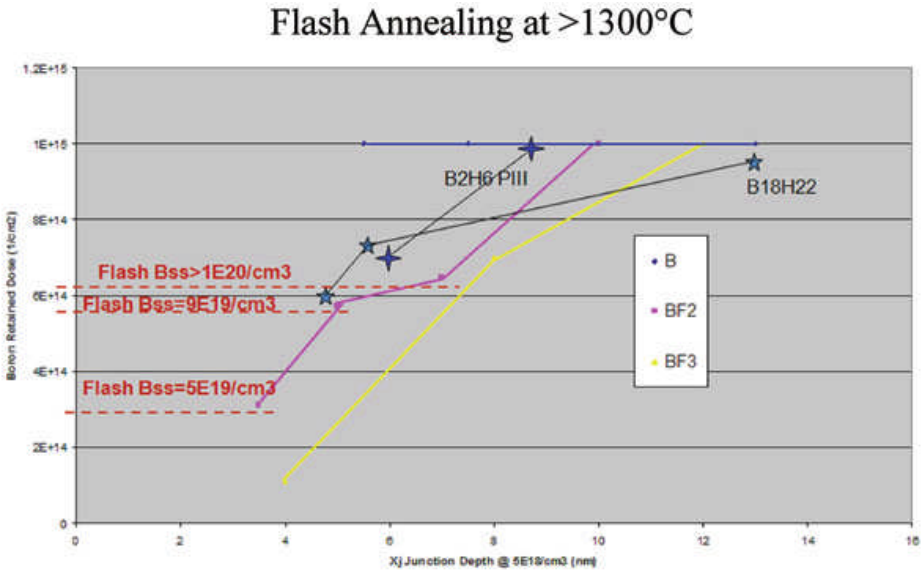
1. The DRAM dual poly gate (DPG) structure requires a compensating very high-dose boron implant in the 1×10^{16} to $1 \times 10^{17}/cm^2$ dose range. The process choices are $B_{18}H_{22}$ molecular implant in the $1\text{-}3 \times 10^{16}/cm^2$ dose range on traditional beam-line HC implanters, or plasma implantation in the $1\text{-}2 \times 10^{17}$ $/cm^2$ dose range using BF_3 or B_2H_6 source materials.
2. The 32 nm node ultrashallow junction (USJ) doping requirement of 50-100 eV equivalent energy for boron while maintaining a retained dose of $1 \times 10^{15}/cm^2$. The 50-100 eV equivalent energies can be realized by using molecular dopant species like $B_{18}H_{22}$ for p-type dopant and P_4 or As_4 for n-type dopant using the ClusterIon source on traditional HC implanters.

Compensating p+ DPG doping — For a 60 nm thick poly gate, a 3.5 keV boron equivalent energy is desired.[5] With plasma doping, the dopants are piled up at the surface and decline exponentially in depth. Beam-line implantation produces the classic Gaussian-like profile, where the majority of the dopant is deeper and retrograde at the surface. Comparative examples of these profiles are shown and reproduced in Figure 1a as-implanted and Figure 1b post-anneal.[6] Decel-mode beam-line implantation cannot be used, because any boron energy contamination will penetrate through the gate and add dopant to the channel region. Plasma doping has additional issues, such as BF_3 plasma etching the silicon while B_2H_6 plasma leads to surface deposition. However, both plasma doping and beam-line implantation with $B_{18}H_{22}$ are being used for DPG manufacturing starting at the 70 nm DRAM node.[7,8]



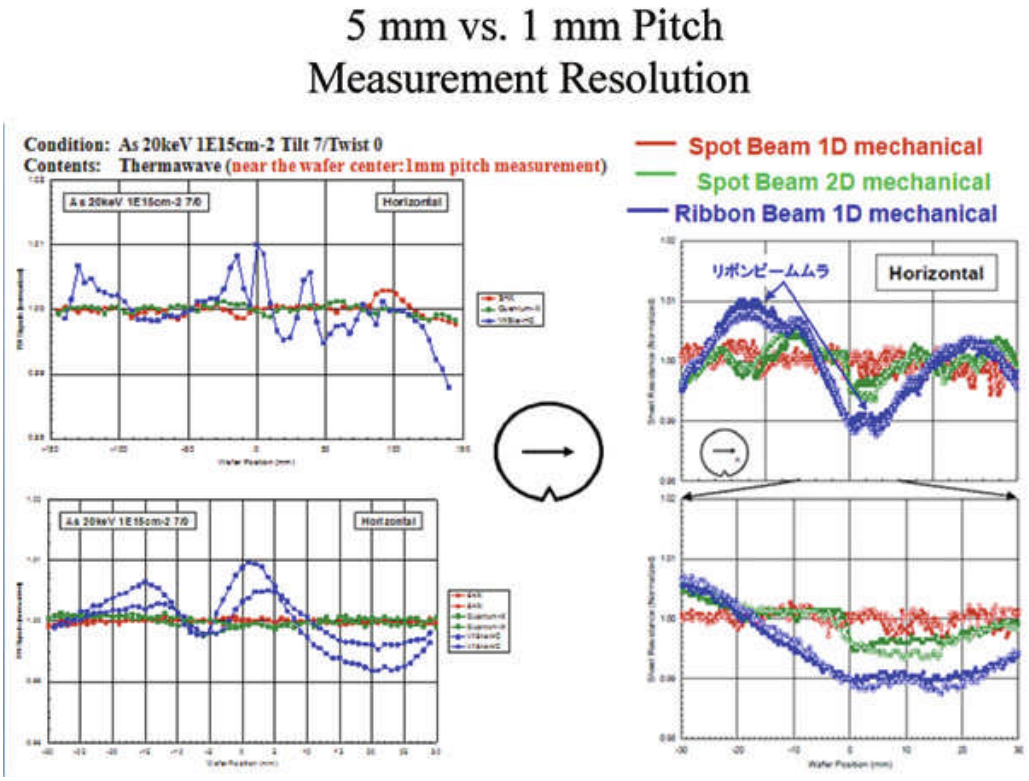
1. SIMS dopant depth profile comparison between beam line and plasma doping as implanted (left) and after anneal (right).[6]

USJ — For the 45 nm node, the X_j target is 12-20 nm, requiring boron energy to be 200-500 eV. However, for 32 nm node USJ, the targeted X_j is between 8-15 nm after anneal. This drives the boron implant energy down to between 50-100 eV, which would produce an as-implanted X_j=5-6 nm if a pre-amorphizing implant (PAI) is used to prevent boron dopant channeling. In this range, conventional HC tools must use decel-mode, which leads to energy contamination. The shallow junction requirement places tight constraints on allowable energy contamination — usually <0.1% — constraining decel tools to low decel ratios — typically <3 to 1. The BF_2 option would require energy in the range of 250-500 eV, but residual implant damage, end of range (EOR) defects and other adverse effects of fluorine make this option less desirable.[9] Using $B_{18}H_{22}$, the operational energy would be 1-2 keV in drift mode, avoiding the defect issues with BF_2 and PAI+B implants. Another issue for junctions below 10 nm is the retained boron dose after implant and annealing (Fig. 2).[10] The boron solid solubility (B_{ss}) activation data shown is for flash annealing at >1300°C, where an activation level of 1×10^{20}/cm^3 is realized until the retained dose drops below 6×10^{14}/cm^2. With a retained dose of 3×10^{14}/cm^2, an activation level of only 5×10^{19}/cm^3 is realized for BF_2; therefore, at low energies, retained dose and total activation levels vary with each implant technology. Since enhanced boron dopant activation was reported when using $B_{18}H_{22}$ with advanced annealing techniques such as flash, laser and solid-phase epitaxial (SPE) retained dose may not be a major concern as it is with BF_2.[9]

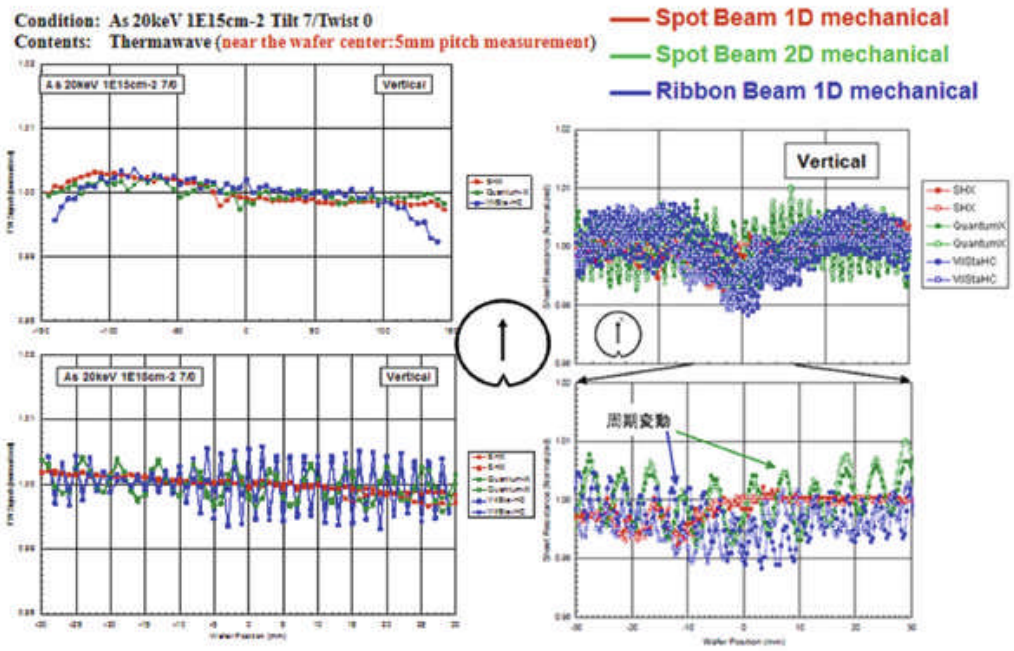


2. Retained dose for boron for various junction depth and dopant species.[10]

Serial HC implanter design —Single-wafer HC implanter replaced batch type because of gate poly yield failure.[11] Each HC implant vendor has a different serial wafer end station design, including scanning mechanism resulting in a unique non-uniformity signature caused by local and global variation in implant precision due to dose and angle control. Any variation in localized implant angle results in asymmetrical transistor, V_t, and gate length variation and gate delay degradation.[4] Detecting these localized implant micro variation with HC implantation requires 0.05-0.1 mm pitch metrology tool resolution. Figures 3 and 4 show thermawave results with a 5 mm vs. 1 mm pitch measurement resolution for three different serial HC implanters. Note that a left to right variation signature pattern can be detected on the ribbon beam implanter with either the 5 or 1 mm measurement pitch in Figure 3, while top to bottom line scans showing a 2 mm variation in localized implant uniformity for the ribbon beam and a 6 mm variation in localized implant uniformity for the spot beam 2-D mechanical scan HC implanters could not be detected with the 5 mm measurement pitch, requiring the 1 mm pitch shown in Figure 4. For more detail, a 0.1 mm, or even a 50 µm, pitch measurement for detecting these micro variations is required. Sheet resistance (R_s) measurements by 4PP with a 1 mm pitch resolution are also shown in Figures 3 and 4, depicting good correlation to the thermawave micro variation results. Photoluminescence wafer imaging (PLi) maps and diameter scans for two other similar serial HC implanters (ribbon beam and spot beam with 1-D mechanical scan) are shown in Figure 5, and their unique local micro variation signatures can also be detected for the two different mechanical scan methods.

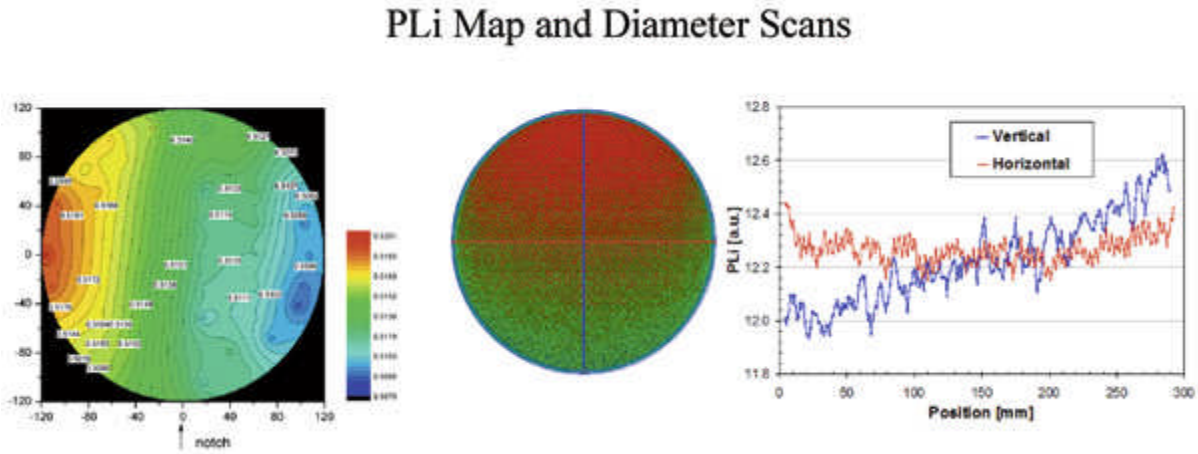


3. Left to right thermawave and 4PP line scans with 5 mm vs. 1mm pitch resolution comparing three different serial HC implanters.



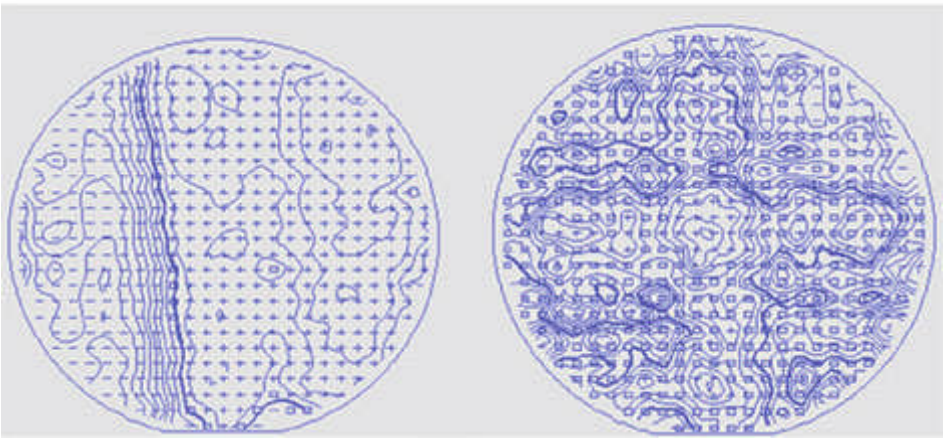
4. Top to bottom thermawave and 4PP line scans with 5 mm vs. 1 mm pitch resolution comparing three different serial HC implanters.

Global variation can be reduced but not eliminated by going to quad-mode or even tilted implantation.[12] Adding quad-mode implantation changes the global variation signature from a paintbrush-like striping left to right with ribbon beam to a four-leaf clover-like fourfold symmetry pattern, as shown below in Figure 6 using thermawave analysis. For spot beam with 2-D mechanical scan, uniformity can be improved by changing the beam spot size and number of scans (scan pitch).



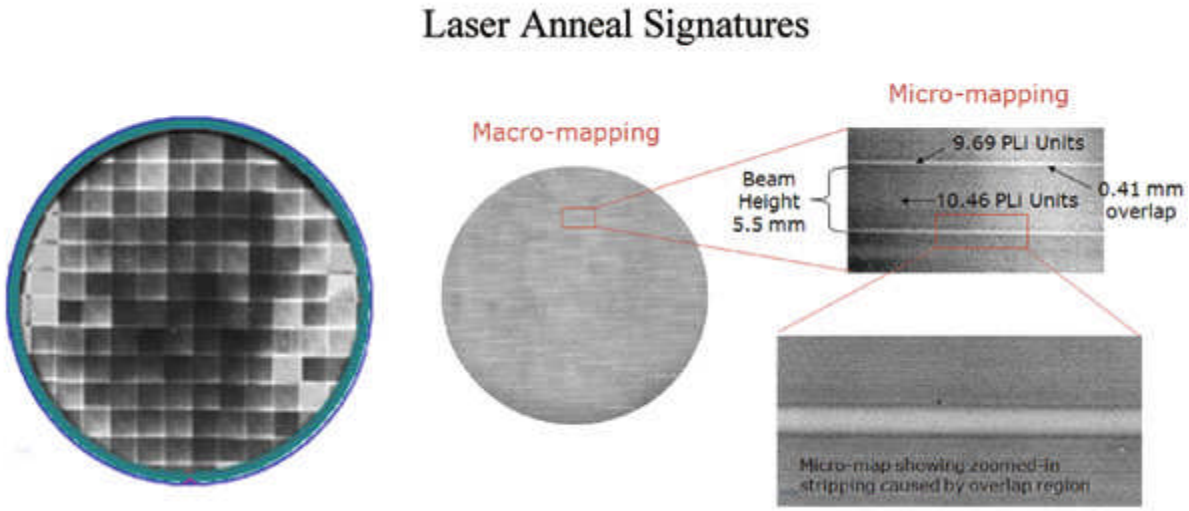
5. PLi showing full wafer imaging and diameter scans for ribbon beam (left) and spot beam (right) with 1-D mechanical scan.

When the electrical dopant activation level (B_{SS}) is 10-100× below the chemical level, dose variation is not critical — this is especially true for boron. With arsenic, this difference is only about 2-5×. Also, with soak or spike rapid thermal annealing (RTA) with >15 nm of dopant diffusion, the as-implanted non-uniformity is washed out. Although, with diffusion-less activation, the as-implanted signature becomes the final after-anneal signature, so detection and monitoring of these effects is important. It is important to know the diffusion-less activation annealer signature, which can also contribute to both global and micro-localized device variation for flash and laser annealing (Figs. 7 and 8).



6. Ribbon beam: single scan implant direction (left) and quad-mode implant (right).

Besides the different unique serial implant signatures discussed above, millisecond flash and laser annealing equipment also has unique annealing non-uniformity signatures (Figs. 7 and 8). PLi shows the signature of each xenon lamp in Figure 8a, and the EM-4PP R_s diameter line scan measurement is shown in Figure 8b. Localized variation in arsenic dopant activation (R_s) caused by the lamp signature can be ~23%. Improvements are being made by design changes, such as better multi-zone heater control for uniform thermal heating across the wafer in combination with lower-temperature spike annealing, and this can reduce wafer global variation by 4× and local micro variation by 3×.

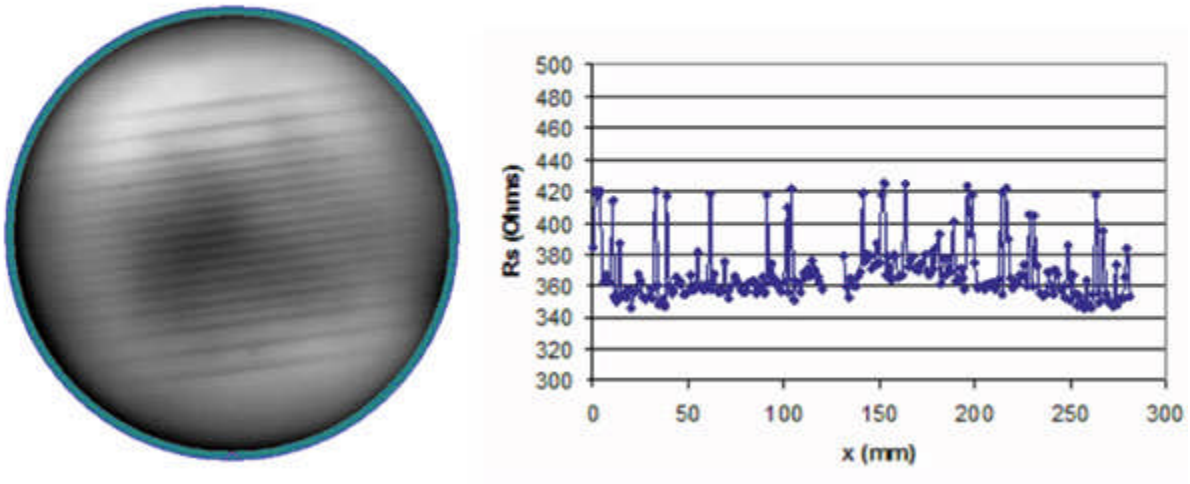


7. Unique laser annealing signatures step and repeat laser annealer A (left) and scanning spot beam laser annealer B with 0.4 mm overlap (right).

Medium current

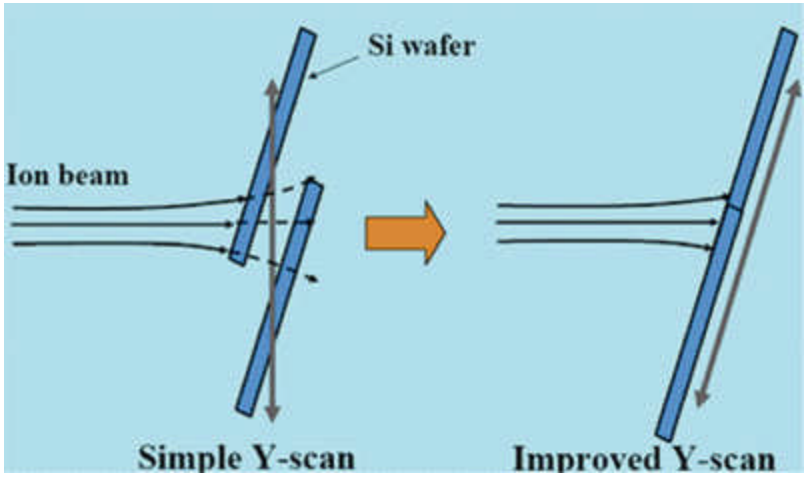
Medium current implanters make up ~31% of the total implant market, and implant equipment vendors are pushing both the high- and low-energy limits. Over the past few years, the upper-energy limit for charge state 3 (X+++) has increased from 750 to 900 keV for retrograde n-well implants, while the lower-energy limit went from 5 keV to 500 eV to meet the lower-energy requirements for HALO and pocket implants.

At energies below 5 keV, beam blowup can be an issue, showing 150 mm spot beam size for boron at 5 keV, while switching to $B_{10}H_{14}$ reduced the beam spot size to only 10 mm.[13] Similar improvements can also be realized with $B_{18}H_{22}$. At high tilt angles, the on-wafer beam spot size could change significantly, resulting in a huge variation of dopant precision (angle and dose) across a 300 mm device wafer. The implantation shadowing effects caused by the gate stack structure during the HALO or pocket high-tilt implant result in top to bottom across-wafer device variation (Fig. 9).[14]



8. Flash Xe lamp annealed n+ arsenic implant showing lamp signature and localized variation in dopant activation level PLi wafer map image (left) and EM-4PP diameter line scan showing Rs variation (right).

Using isocentric scanning to maintain constant focal length is one solution. Another option is to use higher mass dopant species, such as molecular dopant species ($B_{10}H_{14}$, $B_{18}H_{22}$, As_4 and P_4), or indium and antimony, which would require higher-energy implants, avoiding beam blowup. However, indium and antimony dopants may lead to residual implant damage and end-of-range (EOR) defects that degrade junction quality/leakage with millisecond annealing. As the industry moves to diffusion-less annealing starting at the 45 nm node, multiple HALO implants will be used for precise short channel effect (SCE) and gate length control, requiring extreme implant precision with minimal variation (Fig. 10).[15] Similarly, multiple tilted extension implantations are being studied for SCE optimization with diffusion-less activation, leading to lateral graded single-source drain structures.[16]

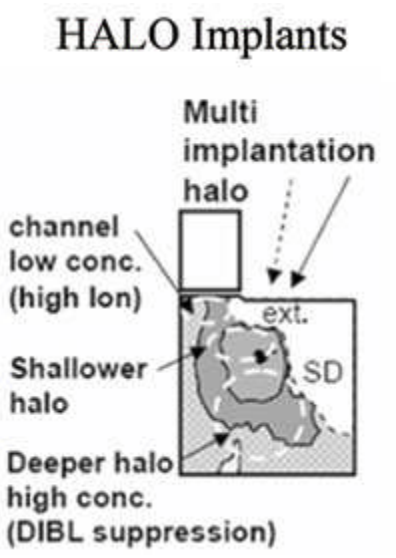


9. Isocentric scanning results in constant focal length and spot beam size during high-tilt implants with gate stack shadowing effects.[14]

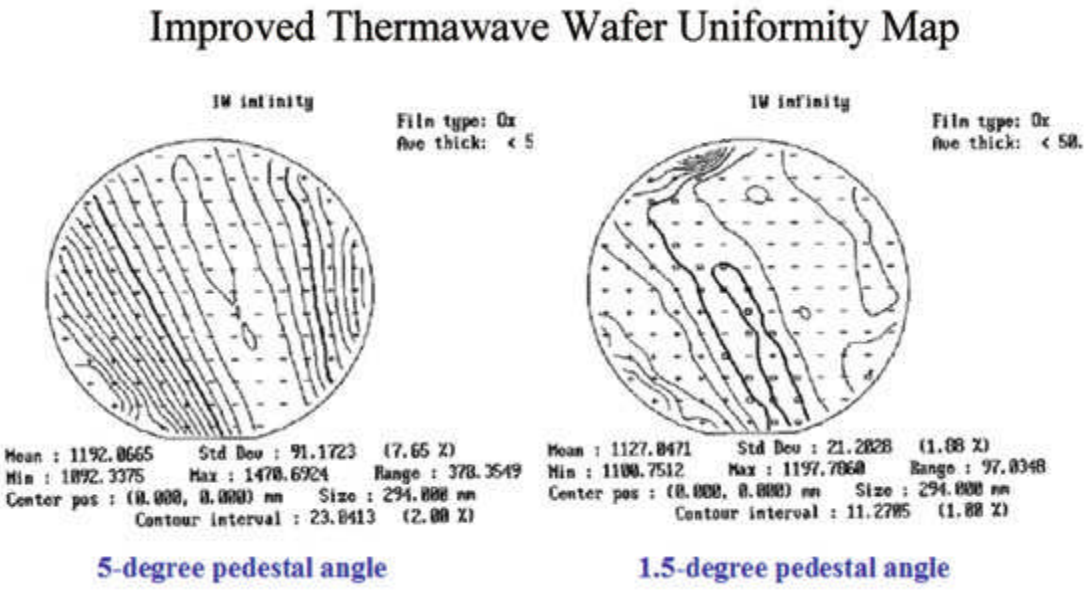
High energy

For the past five years, the HE market has remained steady at 17-18% of the total implant market, and has not declined as many thought it would. Silicon on insulator (SOI) is still a small market, and bulk silicon still dominates today, requiring both shallow and deep retrograde wells. Also, the increased demand worldwide for DRAM, flash and embedded memory chips using deep MeV twin- and triple-well structures, as well as increased CMOS imager device demand with deep dopant structures, continue to require MeV implant energy range. The dominant HE implanter design is still batch wafer type with a market share of 85%, even though single-wafer HE implanter was first introduced in 2000. For some unique imager device design, super MeV implanters with energy range 4-8 MeV are used.[17]

Single-wafer HE implanter design is not required today because there are no poly gate patterned structure present for well doping, therefore ballistic particle impacts are not device yield failures as they are with HC implanters, which drove the industry to switch from batch to serial HC at the 65 nm node.[11] Batch cone-angle effect on HE implant precision leads to across-wafer variations in devices.[1,2] However, the cone-angle effects on dopant profile depth variation across the wafer caused by channeling and de-channeling can be minimized by switching from a 5° cone-angle disk to <2° or by using thicker screen oxides >12 nm.[18,19] Note the improved thermawave wafer uniformity map of 1.88% with the 1.5° pedestal compared with the 7.65% variation with the 5° pedestal for a P+ 500 keV/3 × 10^{13}/cm^2 implant without screen oxide (Fig. 11). Figure 12 shows the SIMS dopant depth profile across a wafer using the 1.5° disk where no variation in the depth profiles can be detected for the phosphorus 500 keV 2 × 10^{13}/cm^2 implant without screen oxide. This reduces V_t variation caused by variation in the near-surface well dopant profile. Results comparing no screen oxide to 10 and 20 nm screen oxide with the 1.5° disk is shown in Figure 13 for thermawave and R_s uniformity. With the thicker screen oxide >10 nm thick, the thermawave uniformity improves from 1.8% down to <0.8% and 0.6%, respectively, which is within 0.1-0.2% of single-wafer HE implanters.

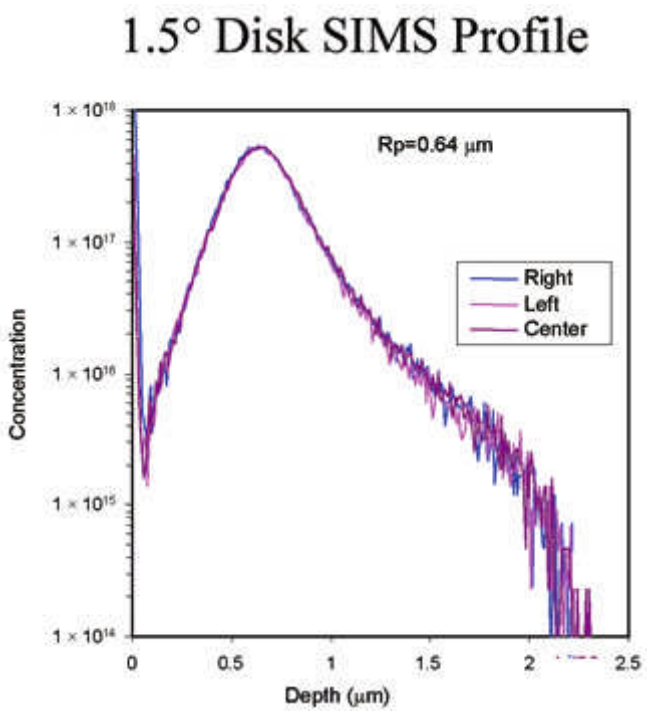


10. Multiple HALO implants to control SCE with laser annealing processing.[15]



11. Thermawave uniformity comparison between 5°and 1.5° batch disk cone angle.

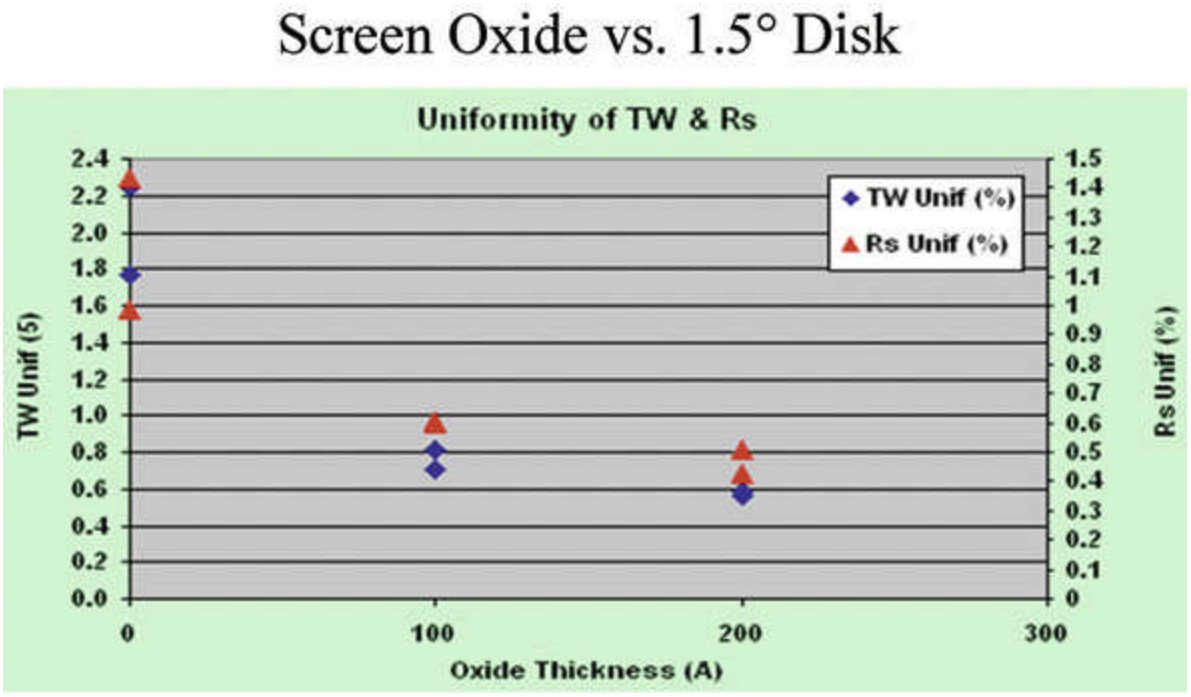
The other effect of cone angle is on photoresist shadowing, but, at such high energies, lateral straggle can be significant and override photoresist implant shadowing effects when using a 1.5° cone-angle batch disk with 45° wafer-twist orientation, so only the square root of two (0.717) of the sine-angle effect is left (1.5° reduced to 1.05°). Therefore, with a 2-µm-thick photoresist, 45° wafer rotation and 1.5° disk, the lateral encroachment is reduced from 52.3 to 36.6 nm. Lateral straggle for boron and arsenic at 100 keV will be ~60 and 15 nm, respectively, so for boron, lateral dopant straggle determines lateral dopant position, and angle precision is not critical.[20]



12. SIMS across wafer dopant depth profile for the 1.5° disk.

Summary

HC implanters are now all single wafer, but they all have a unique, correctable, dopant micro-variation signature that can only be detected and monitored with <0.1 mm pitch spatial resolution. The various advanced millisecond annealing equipment have unique micro and macro annealing variation signatures that can either add to or hide the implant dopant variations, so new metrology techniques with <0.1 mm step resolution are needed.Medium-current implanters have extended their upper-energy range to 900 keV and lower-energy range to 500 eV. For high-tilt implantation, precision will require constant focal length and, therefore, isocentric scanning motion and higher mass dopant species implants to achieve retrograde and dopant-free channels with diffusion-less annealing techniques. HE implanters will all be single wafer later this year.



13. Effects of screen oxide thickness with the 1.5° disk on TW and Rs uniformity.

Acknowledgements

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References

1. D. Kapila et al., "Deterministic Spatial Variations In Retrograde Well Implants ," *IEEE Trans. Semi. Manu.*, 1999, Vol. 12, No. 4, p. 457.
2. 2. K. Min et al., "Estimation of Tilted Wafer in Ion Implantation Process," IIT, 2000, September 2000, Section P2-22.
3. 3. K. Yoneda and M. Niwayama, "The Drain Current Asymmetry of 130nm MOSFETs Due to Extension Implant Shadowing Originated by Mechanical Angle Error in High Current Implantation," IWJT, 2002, Section S2-3, p. 19.
4. 4. T. Kuroi and Y. Kawasaki, "Ultra-shallow Junction Formation for 45nm node and beyond," USJ, 2005, p. 4.
5. 5. T. Parrill and L. Rubin, "Transistor Scaling is Moving Implant Energies Lower ," *Solid State Technology*, June 2005, p. 61.
6. 6. S. Qin and A. McTeer, "Device Performance Evaluation of PMOS Devices Fabricated by B2H6 PIII/PLAD Process on Poly-Si Gate Doping," IWJT, 2006, p. 68.
7. 7. "Industry-Leading Memory Manufacturer Selects VIISta PLAD for High-Dose Dual Poly Gate Implant ," Varian Semiconductor Equipment Associates Inc. Press Release, July 25, 2006.
8. 8. "Axcelis Announces Key Design Win at Major Asian Memory Chipmaker for New Optima HD Imax Molecular Implant System," Axcelis Technologies Inc. Press Release, Oct. 3, 2006.
9. 9. J. Borland et al., "High Dopant Activation and Low Damage p+ USJ Formation," IIT, June 2006.
10. 10. J. Borland, "Process Variability Reduction For Gate Doping and USJs ," *Semiconductor International*, December 2006, Vol. 29, No. 13, p. 49.
11. 11. Y. Kawasaki et al., "The Collapse of Gate Electrode in High Current Implantation of Batch Type," IWJT, 2004, p. 39.
12. 12. Y. Eurokin and J. Liu, "Precision Implant Requirements for SDE Junction Formation in Sub-65nm CMOS Devices," IWJT, 2006, p. 21.
13. 13. T. Aoyama et al., "Decaborane Ion Implantation for sub-40nm Gate Length PMOS-FETs to Enable Formation of Steep Ultra-shallow Junction and Small Threshold Voltage Fluctuation," IWJT, 2005, Section S2-2, p. 27.
14. 14. K. Suguro, "Prospects and Challenges in USJ Technologies For Next Generation LSIs," vTech presentation, July 2005.
15. 15. M. Narihiro et al., "Sub-30nm MOSFET Fabrication Technology Incorporating Precise Dopant Profile Design Using Diffusion-less High Activation Laser Annealing," IEEE RTP, October 2006, p. 147.
16. 16. J. Borland, V. Moroz, H. Wang, W. Maszara and H. Iwai, "High-Tilt Implant and Diffusion-less Activation for Lateral Graded S/D Engineering ," *Solid State Technology*, June 2003, p. 52.
17. 17. J. Borland and N. Tokoro, "Consumer Demands Make For A Sizzling Imaging Market In Japan ," *Solid State Technology* , November 2004, p. S18.
18. 18. Y. Kawasaki et al., "The Angle Control Within a Wafer in High Energy Implantation of Batch Type," IWJT, 2002, p. 15.
19. 19. C.P. Chang et al., "Enabling Shallow Trench Isolation for 0.1um Technologies and Beyond," VLSI Symp., 1999, Section 11B-4, p. 161.
20. 20. L. Rubin, "Angle Control in High Current Ion Implanters ," *Solid State Technology*, October 2002, p. 39.