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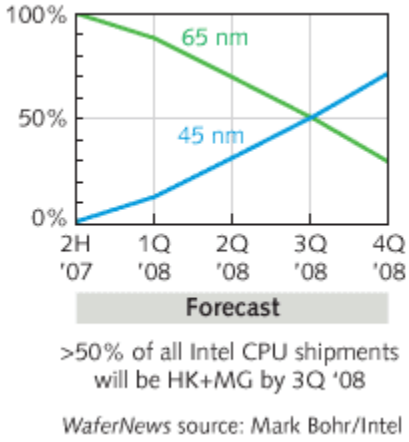


VLSI SYMPOSIUM REPORT: Devicemakers lift hoods to finally reveal HK+MG work

by John Borland, contributing editor, Solid-State Technology

The VLSI Symposium meeting this year (June 12-14, Kyoto, Japan) revealed there will be not one, but many different solutions for the production implementation of hafnium-based oxides at the 45nm node and beyond, with Hf-based dielectric *k* values varying from a "medium"-*k* (8-12) up to a true high-*k* of 22-24. The gate electrode for some companies will remain poly, while others will use a very thin metal/thick poly stacked layer (metal inserted polystack, "MIPS") and others will use a metal-only electrode. If metal is used, it can be single metal, or dual metal for nMOS and pMOS.

Various gate process flow integration approaches will also be used: gate-first; gate-first, but with disposable spacer (reverse source drain); gate-last (replacement gate); and a hybrid of gate-first for one type of MOS transistor, and gate-last for the other type of MOS transistor. The question is, how long can the industry support these multiple approaches? Some technologist say they must converge by the sub-32nm node, while others feel it may never converge.

Handicapping the HK+MG field

Technologists from Intel, NEC, IBM, Toshiba, Samsung, and SEMATECH participating in an evening panel discussed the status and prognosis for high-*k*/metal gate (HK+MG) transistors, suggesting that there will be many different solutions for high-*k* with *k*-values varying from 8-24 in combination with gate electrodes including poly only, poly/metal stack, or pure metal -- though interestingly, however, no one on the panel mentioned fully silicided (FUSI) as an option for metal gate.

Mark Bohr, Intel senior fellow in logic technology development, listed Intel's key HK+MG milestones, going back to late 2003, spanning early work on 45nm SRAMs to earlier this year touting working HK+MG processors. Main issues with gate-first are temperature restrictions and etching control of two different metals for nMOS and pMOS at the same time (the company uses ALD for control of thickness), he noted, adding that gate-last makes the process very flexible but requires new process flows. A third option, suggested by Mark Bohr, is a "hybrid" that allows gate-first for one type of MOS transistor, and gate-last for the other type of

MOS transistor, providing more flexibility for process optimization. For all three models, the best flow is the one that works, he noted.

Bohr said he believes the industry will see all three options over the next few years, until the industry perhaps converges on one approach. He also pointed out that HK+MG will crossover to become >50% of Intel's CPU shipments by 3Q08 *(see chart above)*, perhaps less than a year after entering into mass production. Bohr also noted that HK+MG adds 4% total wafer processing costs, the cost of metal + via layer, or 1/3 the cost of SOI wafers. The biggest benefit Intel sees with HK+MG is power reduction, with 1/10 the gate oxide leakage compared to 65nm with SiON and 1/5 the source drain leakage *(see chart below)*. The second-largest benefit is seen to be a performance increase (20% higher drive current), followed by scaling.

K. Imai of NEC noted that his company introduced high-*k* with poly at the 55nm node for LSTP devices, but that metal will not follow until 2009. They use gate-first, and believe work function tuning is the No.1 issue, with FUSI pattern dependency also a concern. With gate-last, though, the only issue is CMP, which is an easy, but more complex process, he indicated. Therefore, he said, NEC uses poly/HfSiON for nFET and poly/TiN/HfSiON for pFET transistors.

Samsung's U-I. Chung said that gate-first is the only option for memory for self aligned contacts, and he sees three possible gate-first approaches for DRAMs. Option No.1 is dual poly gate, and would use high-*k* gate dielectric with n+ and p+ poly electrodes (no metal). The second option is single metal gate, using HK+MG for pMOS and high-*k*/n+ poly for both nMOS and cell transistors. Option No.3 is a dual metal gate approach, with HK+MG#1 for pMOS and HK+MG #2 for nMOS, with the gate-first approach.

With respect to the use of MOCVD, Chung noted that Samsung uses MOCVD for >1.2nm EOT and ALD for less than 1.2nm EOT. The Toshiba panelist, Y. Tsunashima, added that his company utilizes MOCVD for >1nm EOT and ALD for less than 1nm EOT.

Mukesh Khare, senior manager of IBM Research, explained that gate-last is very flexible, but there are many integration challenges; while the gate-first material challenges, though complicated, are preferred because of the low cost. He prognosticated that 50% of the industry would be using high-*k* by the 32nm node. For details, he pointed to IBM's paper presented later at the VLSI Symposium (11A-1, "High performance high-*k*/metal gates for 45nm CMOS and beyond with gate first processing"), in which researchers reported using a very thin single metal with a very thick poly on top for the HK+MIPS electrode, and said they dope the poly back for the desired n+ and p+ V_t targets. IBM's presentation was different from the published paper, however, most notably in that the spike temperature was >1080°C in the paper, but mentioned as 1000°C in the presentation. Also, in the paper IBM mentioned using spike + advanced annealing, but no mention of msec (advanced) annealing was made in the presentation.

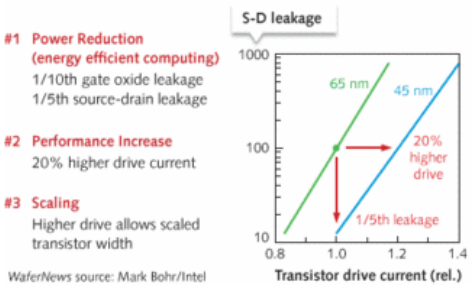
Click here for *WaferNEWS*' exclusive interview with Mukesh Khare, project manager for IBM's HK+MG development, who discusses details of IBM's new "gate-first" HK+MG transistor technology.

In other papers discussed at the VLSI Symposium, Gen Tsutsui of NEC finally revealed the company's Hf-oxide (paper 10A-2, "A cost effective LOP/LSTP integrated CMOS platform utilizing multi-thickness SiON gate dielectrics with Hf for 45nm node"), reporting use of a stacked SiON/Hf dielectric layer with the same Hf deposition on four different SiON thicknesses, to realize EOTs of 1.35nm, 1.75nm, 3.2nm and 7.0nm.

Meanwhile, Renesas reported on using n+ poly/metal/high-*k* for pMOS while nMOS remained poly with an n+ poly/high-*k* (paper 12A-1, "Advanced poly-Si NMIS and poly-Si/TiN PMIS hybrid gate high-*k* CMIS using PVD/CVD stacked TiN and local strain technique"). Unique to Renesas' process is an in situ phosphorus-doped n+ poly for both the nMOS and pMOS poly gate electrode, rather than a separate p+ poly for the pMOS electrode. The researchers also mentioned using spike RTA + laser annealing. -- ***J.B.***

John Borland is founder of J.O.B. Technologies, and a member of SST's *Editorial Advisory Board.*

Next week, WaferNEWS *will report on HK+MG results from the SEMATECH and IMEC consortia, as well as other noteworthy papers disclosed at the VLSI Symposium.*



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