Improving Junction Uniformity and Quality with Optimized Diffusion-less Annealing

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1. Introduction

For the 32nm node the industry will be using: 1) SiON/poly/metal, 2) medium-k (10-12) HfSiON/metal and 3) high-k (20-25) HfO_2/metal gate stack structures. The process integration flow options under investigation are: 1) gate first standard process flow, 2) gate first with disposable spacer process flow and 3) gate last (replacement gate) process flow. The targeted USJ junction depth can range from a conservative 20nm down to an aggressive 8nm. Achieving high quality aggressive junctions <15nm will require diffusion-less or <5nm diffusion annealing techniques. There are numerous annealing options available that is dependent on the gate stack structure and process integration flow so the objective of this study was to determine if we could achieve diffusion-less USJ using: 1) high temperature msec annealing technique, 2) lower spike annealing temperatures and 3) higher SPE annealing temperatures. We also wanted to make sure the annealing technique was "design for manufacturing" which does not increase wafer device variation globally and locally due to annealing micro-uniformity variations.

2. Experimentation

To eliminate any potential global and local micro-variation with the SDE implantation we used a batch high current implanter rather than serial high current implanter for the B and Ge-PAI+B dopant implantation at Selete. Only the $B_{18}H_{22}$ implantation was done on a serial medium current implanter using the Cluster Ion source at Nissin. All processing were done with 300mm wafers and annealed with a 650°C SPE, a 900°C spike or a 1000°C spike anneal in a hot wall RTP system while the Flash anneals were performed in a Xe-lamp Flash annealer at Selete. Full wafer maps and diameter line scans to characterize global and localized annealing micro-uniformity and quality were performed at Nanometrics using the Sipher PLi tool for photoluminence analysis and at Frontier with the RsL tool for sheet resistance and junction leakage measurement while micro-Rs measurements were made at Solid State Measurements using their EM-4PP with 5mm to 0.05mm step resolution.

3. PLi Metrology

The PLi measurement setup principles are illustrated in Fig. 1. The tool is equipped with two different wavelength lasers, called the Channel and the Bulk Probe. Depending on the desired probing volume (implantation energy and dose), the Channel and Bulk Probes are appropriately selected for evaluation. In the lateral dimension, laser beams are focused to a two micrometer spot by a system of lenses. The tool can operate in full wafer and micro mapping modes of operation and is used for nondestructive measurements of as-implanted and annealed, bare and patterned wafers. Due to PLi sensitivity to defect presence, ion implantation dose, energy, specie and implantation process conditions (tool signature) can be ultimately measured at sub-1% variation levels. Doping activation effects, presence of residual defects and annealing quality can be also quantified. Full wafer scanning enables detection of macro-uniformity effects used for process optimization and control on a wafer global level. Micromapping down to submicron scanning resolution is used for detection of lattice-based defects and characterization of damage recovery after subsequent annealing processes. Typical annealing equipment signatures characteristic for SPE, Spike, msec Flash and Laser annealers can be easily assessed. Due to the small size of the laser beam and submicron scanning capability, typical test pads in patterned wafers can be effectively probed.

Simultaneously with the PLi maps, surface reflectivity (SR) maps are also collected. Electrically active defects that are present in the wafer bulk, such as post-implantation damage, lattice disturbances (crystal amorphization) or metal contamination are likely to be detected only in the PL image. Surface defects such as particles, growing faults or etching pits are predominantly seen in SR images.

4. Results

Summary of the results are listed in Table 1 below while Fig. 2 shows the PLi wafer image map results for Flash only annealing for each dopant species studied (B, $B_{18}H_{22}$, As and Ge+B). The unique annealing signature can clearly be seen revealing each individual Xe-lamp from the Flash annealer. Also, initial analysis results from the old flash annealer's global and local micro uniformity variation is shown in Fig. 3 where the Xe-lamp unique signature detected by PLi correlated to Rs localized micro-variation measured by EM-4PP. Fig. 3a shows the PLi wafer map image were each Xe-lamp signature can be clearly detected. A global PLi variation of 11 PLi units or 24.4% and local variation of 1 PLi unit or 2.2% can be detected by the diameter PLi scan shown in Fig. 3b and up to 11 PLi unit drop off occurred in the outer 50mm to the edge of the wafer suggesting severe thermal gradients. The local Rs variation was between 350 to 420 ohms/sq or 20% as detected by the EM-4PP in Fig. 3c with a 5mm step resolution and in Fig. 3d with a 0.05mm step resolution. To improve both global and local uniformity we investigated a 1000°C spike and 900°C

spike 1st annealing followed by Flash annealing. With the lower temperature spike 1st annealing step the boron diffusion can be significantly reduced to <5nm at 1000°C [1] and to zero diffusion at 900°C [2] while enhancing the dopant activation effectiveness of the subsequent Flash anneal [3]. Fig. 4 shows the comparison between the Flash only to the 1000°C spike 1st followed by Flash annealing step. The global PLi variation was reduced by 4x from 23.6% to 7.4% and the localized micro-variation reduced from 3.7% to 1.1%. This reflects an Rs global uniformity improvement of 3x going from 8.5% to 2.8% shown in Table 1. The spike 1st anneal seems to dominate wafer uniformity as shown in Fig. 5 which compares the 1000°C Spike + Flash to a 1000°C Spike only where global PLi uniformity was 7.1% and 9.7% respectively while local uniformity was 1.1% and 1.0%. Further reducing the spike temperature to 900°C maintains a 0.8% local variation but the global is 11.1% suggesting some additional RTA uniformity tuning is needed as shown in Fig. 6.

A summary of both PLi channel and bulk probe results are shown in Fig. 7 for all the dopant species and annealing conditions studied. Lowest PLi values are seen with SPE anneal followed by Flash then 900°C Spike + Flash. The 1000°C Spike and 1000°C Spike + Flash had the highest PLi values and all the $B_{18}H_{22}$ implants had the highest PLi values suggesting highest quality junctions even with the 900°C spike + Flash annealing process. PLi wafer image maps for B is shown in Fig. 8, for Ge+B in Fig. 9, for $B_{18}H_{22}$ in Fig. 10. A plot of sheet resistance (Rs) is shown in Fig. 11 and the lowest Rs value of 498 ohms/sq. is observed with Ge+B Flash annealing but the junction leakage current is degraded by 3 orders of magnitude due to the Ge-PAI residual implant damage and EOR (end of range) defects. This is reflected in the low PLi value of 300. With $B_{18}H_{22}$ the Rs value is 751 and very low junction leakage current therefore the highest quality junction with a PLi value of 1000.

5. Summary

Comparisons between B, Ge+B and $B_{18}H_{22}$ implantations for pSDE were made. With Flash only the localized individual Xe-lamps signature was clearly detected by PLi and Rs measurements. Adding a spike first RTA anneal dramatically improved the global and local micro uniformity variation by 2-3x with either a 1000°C or 900°C spike 1st anneal. The highest quality B junctions were achieved with $B_{18}H_{22}$ for all annealing conditions as verified by PLi value and junction leakage current.

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Table 1: Summary of the RsL and PLi metrology results.

Implant	Anneal	Rs	%	Leakage	PLi	Global [%]	Local [%]
B 500eV	1000 Spike	532	2.6	1.0E-07	1630	10.7	1.0
B 500eV	1000 Spike+FLA	535	2.8	1.0E-07	1623	7.4	1.1
B 500eV	900 Spike + FLA	1248	6.2	1.0E-07	1310	8.9	0.8
B 500eV	FLA	2013	8.5	1.0E-07	488	23.6	3.7
Ge+B	1000 Spike	552	1.8	1.0E-07	1715	13.6	0.8
Ge+B	1000 Spike+FLA	564	1.9	1.0E-07	1650	15.1	0.8
Ge+B	900 Spike + FLA	1211	4.9	1.0E-07	852	92.1	0.3
Ge+B	FLA	498	2.1	1.2E-04	279	1.2	0.2
Ge+B	SPE	898	9.8	1.9E-04	282	1.9	0.4
B18	1000 Spike	588	2.9	1.0E-07	2164	13.0	0.4
B18	1000 Spike+FLA	597	2.9	1.0E-07	2108	16.0	0.4
B18	900 Spike + FLA	1098	2.3	1.0E-07	2165	9.6	0.4
B18	FLA	751	4.2	1.0E-07	1029	38.3	4.7
B18	SPE	1245	1.8	1.0E-07	657	12.3	0.2

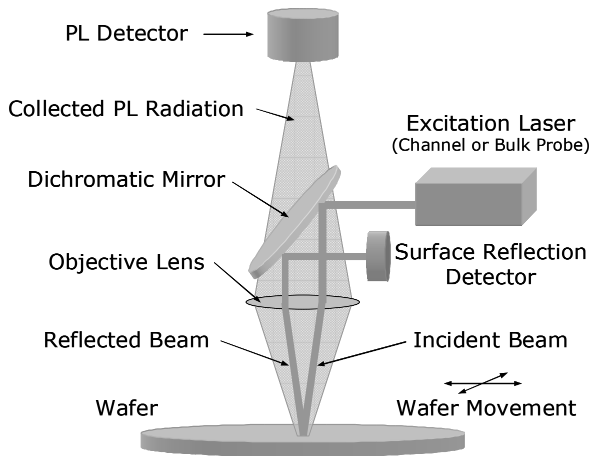


Fig. 1: PLi measurement setup.

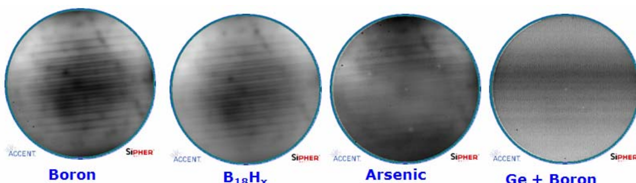
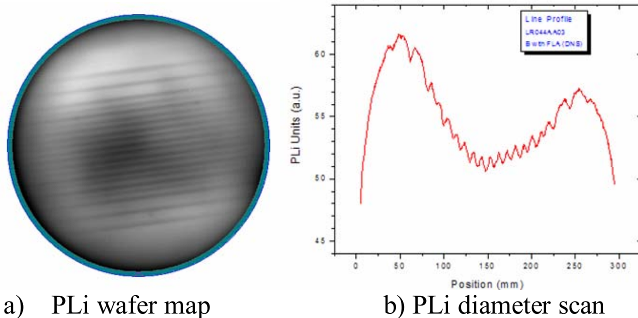


Fig. 2: Flash only annealing PLi wafer image maps for each dopant species.



a) PLi wafer map b) PLi diameter scan

c) EM-4PP with 5mm step d) EM-4PP with 0.05mm step.

Fig. 3: Old Flash annealer global and local micro-variation characterized by PLi and EM-4PP (Rs) showing unique lamp signature.

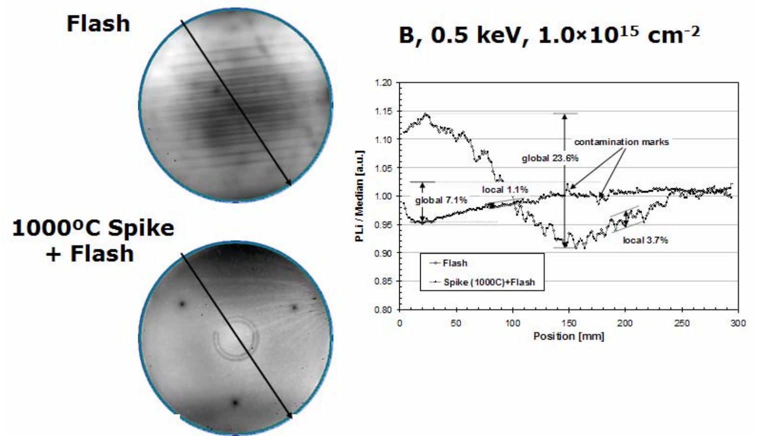


Fig. 4: Comparison of Flash to 1000°C spike 1st plus Flash.

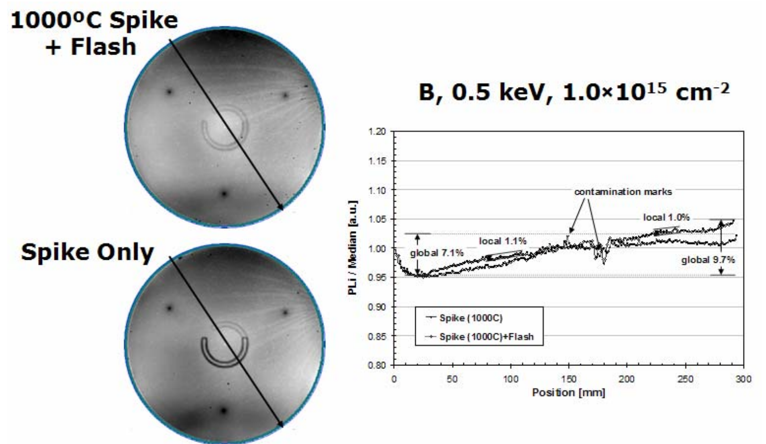


Fig. 5: Comparison of 1000°C spike only to 1000°C spike + Flash.

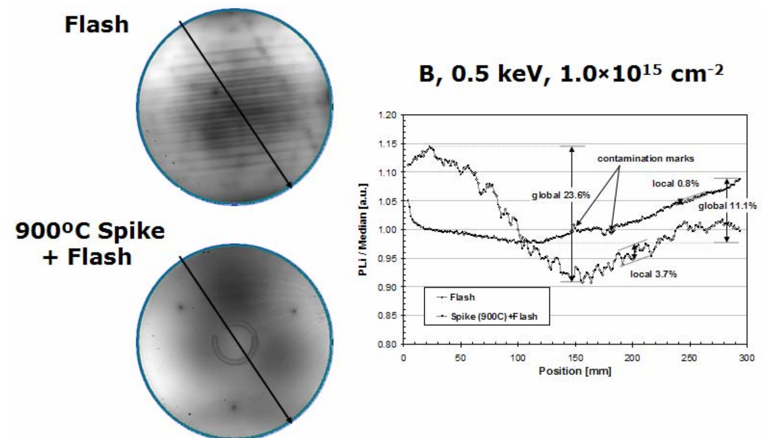


Fig. 6: Comparison of 900°C spike + Flash to Flash only.

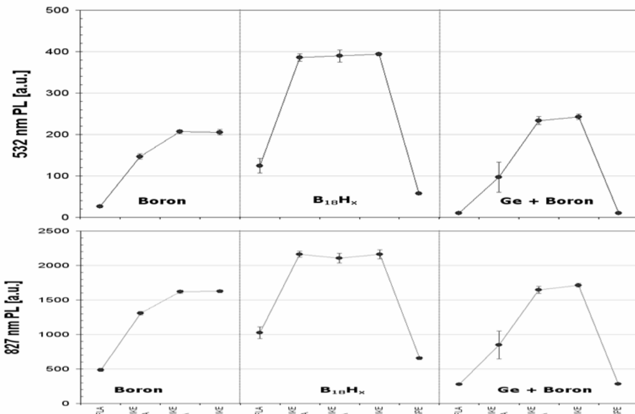


Fig. 7: PLi results comparing surface channel probe to bulk probe.

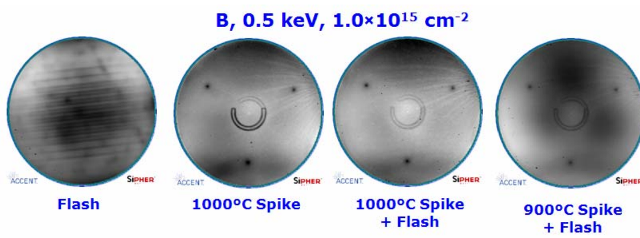


Fig. 8: PLi wafer image maps for B.

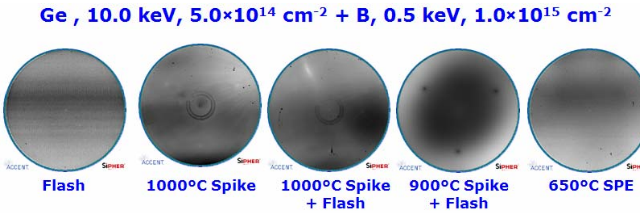


Fig.9: PLi wafer image maps for Ge+B.

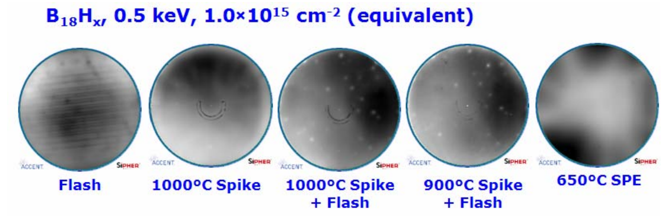


Fig. 10: PLi wafer image maps for $B_{18}H_{22}$.

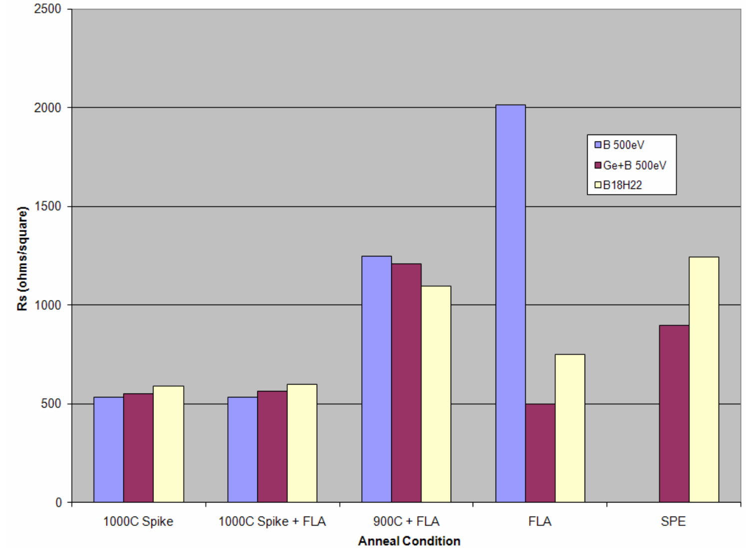


Fig. 11: Rs plot for the various annealing conditions.