Consumer demands make for a sizzling imaging market in Japan

In the 1970s, Japanese IC manufacturers were trying to catch up to the US. In the 1980s, they took the lead and dominated DRAM while the US refocused on logic. In the 1990s, Japanese IC manufacturers lost DRAM dominance to Korea and Taiwan. Now, however, Japanese chipmakers have regrouped and dominate consumer digital electronics and LOP/LSTP logic system-on-chip (SoC) devices for portable communication to satisfy Japanese consumer demand.

The imaging market

The IC industry has been driven the last two decades by PC unit sales, which, in 2004, are expected to reach 185 million units [1]. Cell phones, on the other hand, will reach 620–650 million units this year; with increasing sophistication (especially for flash memory and imaging devices) and capabilities, they are also driving the worldwide IC market, consuming >20% of the worldwide semiconductor total, and growing.

Today, the imaging device market is dominated by Japanese IC manufacturers, who have maintained this leadership role since the late 1980s. In Japan, nearly 100% of all cell phones are sold with still or video imaging cameras, while worldwide, the percentage is only 24.6% (153–160 million units). Worldwide, the digital still camera (DSC) market is expected to reach 75–80 million units [2]. In Japan, 80% of still cameras sold are digital, while only 20% are film, and the current household penetration of digital cameras in Japan is at 30% compared to the USA at only 15%.

The ratio of charge-coupled devices (CCD) and CMOS imagers for 2004 will be ~3.8:1. Only 15% of DSCs are CMOS imagers, and 26% of cell phone cameras are CMOS imagers. Although CCD imaging output will be >140.8 million units and CMOS imagers at 35.2 million units, the greatest growth will be in CMOS imagers where older CMOS fabs can be used as foundries to meet this rapid increase in demand. For this reason, imaging devices are the hottest growing IC market and why Samsung stated it intends to be the no. 3 imager company by 2005 and no. 1 by 2007. The table on this page shows the market share breakdown for cell-phone cameras and DSCs [3].

Market share for cell phone and digital still cameras

	Cell phone cameras (%)	Digital cameras (%)
Sony	–	50
Matsushita	10.7	31.9
Sharp	14	12.7
Fuji Film	–	5.3
Sanyo	16.6	–
Toshiba	16.6	–
Samsung	10.7	–
Others	31.4	0.1

Imaging technology

Consumer digital cameras today have 3–5 megapixels, which equals the quality of film-camera prints. Along with the demand for higher resolution and more megapixels (pixel density increase) comes the miniaturization of each pixel size. The explosive growth for cameras in cell phones with increased resolution is pushing the imaging industry to develop evolutionary designs with improved imaging sensitivity. Also, with improved sensitivity and tailored sensitivity such as to infrared (IR), new applications, such as automotive night-vision imaging and fluorescent dyes to mark specific biological and medical structures where near-IR sensitivity is important, are being realized [4].

Two new methods are being pursued to improve imaging sensitivity. First, super MeV implantation (>4MeV) improves sensitivity, especially in the IR range for new scientific and medical applications of wireless cameras such as internal (to the body) imaging of fluorescently tagged structures by enhancing the IR photon collection for light absorption 10µm deep from the silicon surface.

In 1988, Sony pioneered the use of 2MeV implantation for imaging-device manufacturing. Today, imaging manufacturers are looking at super MeV for energies up to 4MeV or higher. Secondly, new transparent substrate materials such as silicon-on-sapphire (SOS), silicon-on-.quartz (SOQ), or silicon-on-glass (SOG) will allow backside illumination, thereby significantly improving the quantum efficiency up to 95% and eliminating light-scattering interference from multilevel metallization with traditional frontside-.illumination imaging devices.

Frontside illumination improvements

With increased integration of imaging devices and decreased photosensitive area size, both sensitivity and quantum efficiency (QE) of frontside illumination imagers are decreasing. To improve frontside sensitivity, both CCD and CMOS imagers incorporate sophisticated microlensing and light shielding to maximize light directed to the photosensitive area (photodiode) on the imaging device, as reported by Kodak [5]. The researchers reported a 20% improvement in QE with microlensing going from 65% to 85%, as shown in Fig. 1 [4].

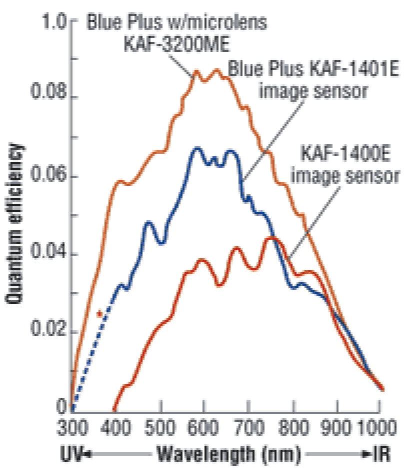

Figure 1. Frontside illumination QE [4].

As the device shrinks, however, more metal layers are used for device integration, especially for CMOS imagers, and the benefits of microlensing diminish due to light interference with the multiple levels of metal interconnection. Figure 2a is an example of four levels of metal as reported by Sony [6]. The stack height of interlevel dielectric (ILD) material for advanced CMOS imagers today can reach 9µm [7], which also limits the metal-layout design flexibility above the photosensitive area to prevent light-scattering transmittance loss. To avoid these light interference/transmittance effects, manufacturers are exploring alternative methods to achieve wafer backside illumination (see Fig. 2b) [6].

Backside illumination: silicon on transparent substrates

The QE of backside illuminated CCDs can be as high as 95%. One problem with this approach is providing frontside wafer mechanical support and strength with easy access to the wafer frontside device metal interconnections. Researchers have proposed forming a glass substrate above the devices on the frontside followed by wafer backside thinning, and then placing the light shields and microlenses on the wafer backside for backside illumination [6]. Figure 2b shows Sony's proposal whereby the light shielding, microlens, and color filters are all on the backside underneath the imaging device; this avoids the multiple levels of metallization interfering with light transmittance to the photodiode area. To improve the light-collection area, Sony also proposed a fan-out structure of a deeper and wider *n*-well under the photodiode, surrounded by a deeper triple *p*-well (Fig. 2b) [6] (refer to "Deep wells" above).

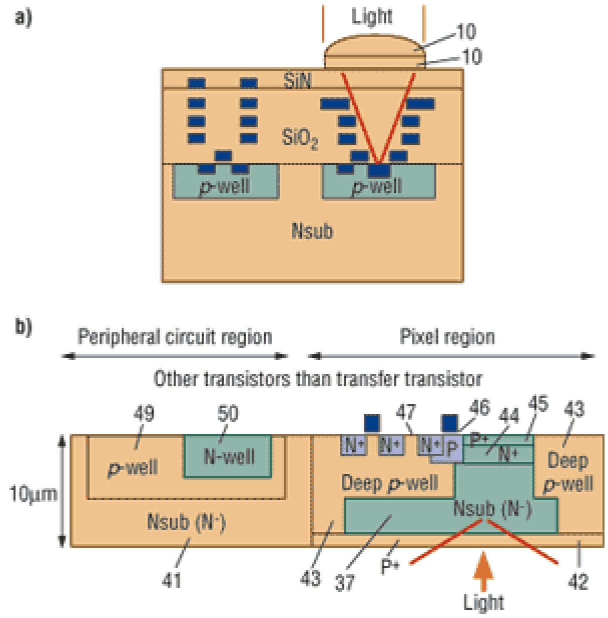

Figure 2. a) Metal layout above the photodiode maximizes light transmittance for frontside illumination in comparison to backside illumination. b) A deep n-well under the photodiode increases the light-sensitive area for backside illumination [6].

With innovative designs in photodiodes that increase the light-collection area, such as the fan-out structure (Fig. 2b), new 3D imaging device configurations — where the photodiode is stacked above or below the transistor — completely avoid microlensing and color filters. In one example, the photodiode is sandwiched between the transparent substrate on the bottom and the CMOS device on the top using a thick (10μm) SOS epi wafer with a thin silicon-layer transfer on top.

Conclusion

With imaging becoming the fastest-growing IC market, and with manufacturing dominance in this sector, Japan's IC manufacturers are well positioned to benefit from the situation. Design innovation, such as 3D imagers with backside illumination, will offer continued imager scaling and increased resolution with more (and smaller) megapixels.

References

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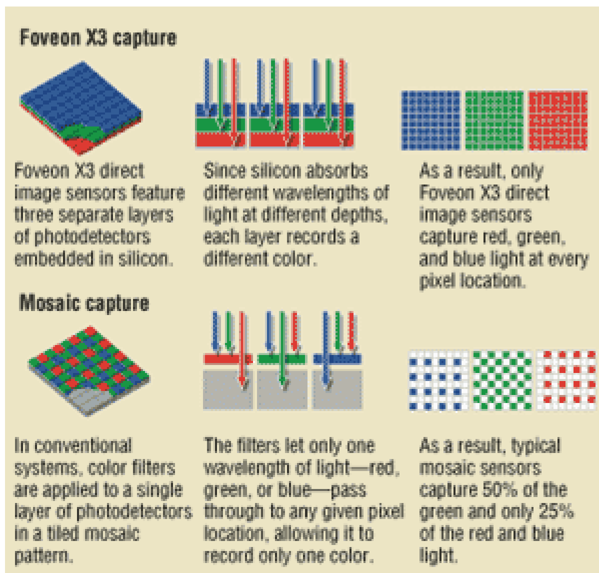
Deep wells

Back in 1988, MeV implantation was first introduced into CCD device manufacturing by all the major Japanese manufacturers using boron up to 2MeV for a deep buried *p*-layer, and P or As up to 1MeV for a deep *n*-sensor. Another benefit of these deep wells or vertical buried photodiodes was reported by Foveon to eliminate the need for the three mosaic separate color filters (red, blue, and green) and layout space as illustrated here [1, 2]. Visible light rays are absorbed in the silicon 5–15µm deep, UV light rays in the 3–7µm depth, and IR light rays 15–50µm deep. In the visible light range, the absorption peak distance difference between blue light (450nm) and green light (550nm) is 0.75µm, and between green light and red light (650nm) is 1.5µm, showing the need for stacked buried photodiodes that can be formed by multiple MeV implantation or double epi buried-layer techniques [1]. The latest generation of imaging devices use super MeV implantation at >4MeV for deeper, multiple vertical-well structures to improve imaging sensitivity and quality.

High-energy implant range for creating deep buried photodiodes

Energy	B (R_p) (µm)	P (R_p) (µm)
500keV	1.0	0.6
1MeV	1.6	1.2
2MeV	2.8	1.8
4MeV	5.1	3.1



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