UNITED STATES PATENT

Granted on October 13, 1998

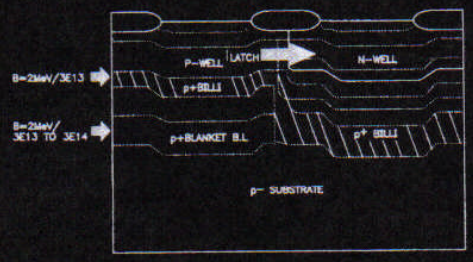
John O. Borland

INVENTOR

5,821,589

METHOD FOR CMOS LATCH-U IMPROVEMENT BY MEV BILLI (BURIED IMPLANTED LAYER FOR LATERNAL ISOLATION) PLUS BURIED LAYER IMPLANTATION

The United States of America



1. A semiconductor device comprising in combination

a p-substrate having an impurity concentration of 10^{15}/cc and a surface having at least one field oxide area

a retrograde n-well therein having a high concentration portion having a concentration of about 10^{18}/cc extending between a depth of 1 micron and a depth of 2 microns, and extending parallel to said surface from a point under said field oxide area in a first direction, and

a BILLI p+layer therein having a concentration of about 10^{18}cc.

The Commissioner of Patents and Trademarks has received an application for a patent for a new and useful invention. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law. Therefore, this

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Grants to the persons having title, the right to exclude others from making, using or selling the invention throughout the United States of America for the term of the patent.

Bruce Lehman — Marcia S. Campbell

Commissioner of Patents and Trademarks — Attest: