

THE UNITED STATES OF AMERICA

UNITED STATES PATENT

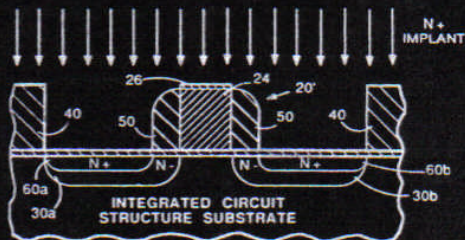
John Borland

INVENTOR

4,975,385

METHOD OF CONSTRUCTING LIGHTLY DOPED DRAIN (LDD) INTEGRATED CIRCUIT STRUCTURE Israel Beinglass, Sunnyvale; John Borland, San Jose, both of Calif. Assignors to Applied Materials, Inc., Santa Clara, Calif.

An improved method is disclosed for forming one or more N- LDD regions in an integrated circuit structure wherein there is no offset between the gate electrode and the source and drain regions in the resulting structure which comprises the steps of: forming a polysilicon gate electrode over a semiconductor wafer substrate, N- doping the substrate to form one or more N- LDD regions, selectively depositing polysilicon on the polysilicon sidewalls of the gate electrode, and then N+ doping the substrate to form N+ source and drain regions in the substrate using the selectively deposited polysilicon as a mask over the N- LDD regions previously formed in the substrate.



ATTEST:

Handwritten signature of Rosella Ahila

ATTESTING OFFICER

In testimony whereof I have hereunto set my hand and caused the seal of the Patent and Trademark Office to be affixed at the City of Washington this fourth day of December in the year of our Lord one thousand nine hundred and ninety and of the Independence of the United States of America the two hundred and sixteenth

Handwritten signature of Harry F. Mansbach, Jr.

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