Smartphones: Driving Technology to More than Moore 3-D Stacked Devices/Chips and More Moore FinFET 3-D Doping with High Mobility Channel Materials from 20/22nm Production to 5/7nm Exploratory Research

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3-D bulk-FinFET at 22nm node uses (551) 8º tapered Fin sidewall with 45º high tilt implantation for doping, eSiGe S/D for PMOS channel compressive strain and amorphous implant SPC (solid phase crystallization) dislocation defects for NMOS channel tensile strain. For 14nm node taller Fins with vertical sidewalls and partial recess embedded n+ S/D was added. 7/10nm node will use direct high mobility channel materials 50% SiGe to 100% Ge. To avoid CVD Ge or SiGe epi defects liquid phase crystallization (LPC) by laser melt annealing is an alternative using amorphous-Ge dose control deposition by ion implantation and at 5nm node gate-all-around (GAA) nano-wire. Residual implant damage into Ge material creates high level of acceptors up to 7E19/cm^3 requiring high temperature annealing above 600ºC to annihilate and establish stable p+ or n+ dopant activation for ultra-shallow junctions. For USJ n+ junctions in Ge, melt controlled junction depth using Sb dopant results in highest dopant activation >1E21/cm^3 at sub-10nm junction depth. Si-capping layer offers lowest n+ Ge junction leakage and Sn co-implantation enables surface strain-Ge engineering for higher channel mobility.

Introduction

Today smartphone ICs are driving technology to More Moore 3-D device scaling and More than Moore 3-D stacked devices/chips with >1.24B smartphones sold in 2014 accounting for >27% of all ICs. The expected increase in smartphone application processor (AP) demand in 2015 (Samsung Exynos 7 for Galaxy S6 and Apple A9 for iPhone 6s) is driving the rapid ramp to 14/16nm technology node "*More Moore*" 3-D bulk-FinFET devices at foundries and "*More Than Moore*" 3-D stacked devices/chips for cell phone cameras and memory devices. Intel was first to production with 3-D bulk-FinFET devices at the 22nm technology node in 2011 and reported their SoC version for Chinese low-end smartphone market and Windows/Nokia smartphones. Intel's 2nd generation bulk-FinFET devices at 14nm node was introduced in Aug 2014 with their SoC version reported in June at VLSI Sym 2015. In Sept 2012 Apple iPhone 5 was first to incorporate Sony's 8M pixel 3-D stacked backside CMOS image sensor for rear-facing camera. In April 2015 Samsung Galaxy S6 incorporated Sony's 16M pixel 3-D stacked backside CMOS image sensor for rear-facing camera and Samsung's 5M pixel image sensor for front-facing camera. Galaxy S6 also introduced 14nm technology node 3-D

bulk-FinFET devices in the Exynos 7 Octa application processor and first 3-D ePOP (embedded package on package) which stacks AP + DRAM (3Gb LP DDR4) + Flash (128/64/32Gb) + eMMC (embedded multi-media card) + controller saving 40% area. Samsung offers 2 versions of their 128Gb NAND Flash memory either as 2-D planar devices using 16nm node process technology or 3-D vertical devices with 32-layers using 40nm node process technology. Toshiba/SanDisk reported their 3-D NAND will use 48-layers. Apple's current iPhone 6 and 6-plus uses A8 application processor with 2-D planar devices using TSMC's 20nm node technology but will change with the introduction of the iPhone 6s in Sept 2015 using the A9 application processor 3-D bulk-FinFET device with Samsung/Foundry 14nm node and TSMC 16FF+ process technology. 10nm technology node is expected in 2016 with higher mobility SiGe or Ge channel material then 7nm node in 2018 and gate-all-around nano-wire by 5nm node in 2020. To understand 3-D FinFET doping and high mobility channel material this paper will first review the current doping and Fin/channel mobility enhancement techniques used for 22nm FinFET production by Intel for both high performance logic and SoC devices and the changes they made for their 2nd generation 14nm FinFET. Then discuss >50%-SiGe to 100%-Ge high mobility channel material formation options for the 7/10nm node leading to 5nm node GAA. Finally a discussion on high dopant activation and low junction leakage ultra-shallow p+ & n+ junctions in high mobility Ge material.

FinFET 3-D Doping Options

For the past decade the industry has investigated various options for 3-D doping of the Fin vertical sidewall. In 2003 Borland (1) reported using high tilt beam-line implantation for lateral graded single source/drain FinFET doping. In 2007 Duffy (2) reported on the limitations of high tilt implantation for FinFET doping being photoresist shadowing limiting implant tilt angle and low chemical retained dose. Photoresist shadowing effects can be solved with thinner resist height and optimized Fin to Fin spacing while electrically active conformal doping is more important than chemical conformal doping and is realized with 45-60 degree high tilt extension implant as reported in 2011 by Mody (3) and in 2009 by Borland (4). When the electrically active dopant solid solubility level in Si is below the chemical dopant level, electrical Fin conformal doping can be achieved and amorphous dopant implant followed by SPC (solid phase crystallization) results in dopant activation level above the solid solubility limit as reported in 2006 by Kennel (5) especially when using msec annealing with amorphous shallow junctions (4). If the implant energy is too high complete amorphization of the Fin may occur resulting in poly-Si crystallization of the Fin after SPC as reported by Beismen (6). This can be avoided by use of lower implantation energy for <10nm shallow amorphous junction formation or tapered Fin sidewall (7). Recently HOT implantation at temperatures >300^{o}C have also been shown to prevent Fin amorphization but this requires a "hard mask" and can degrade NMOS strain-Si technique that relies on amorphization to increase C_{sub} and dislocation defects for n+ S/D stressor with channel tensile strain (8-9).

Plasma implant doping has also been investigated as an alternative to tilted beam-line implant doping over the past decade for conformal doping by numerous companies (10, 11). Results show that plasma doping is actually directional and not conformal and after annealing resulted in severe surface dopant loss up to 97% requiring a surface capping layer before annealing adding process integration steps and costs. Another option is plasma deposition doping of a thin doped layer around the Fin structure

followed by tilted beam-line knock-in implantation called MTI (momentum transfer implant) as 1st reported by Fuse (12) at SSDM-2010 using B or P plasma deposition followed by Ge or Xe tilted knock-in implant. At IEDM-2013 Sasaki (13) reported similar concept using As plasma deposition followed by As +/-7° knock-in implant called IADD (ion assisted deposition and doping). Dopant activation level is limited by solid solubility so a shallow amorphous implanted junction is preferred to achieve highest dopant activation by SPC

Monolayer doping or doped CVD deposited layer followed by dopant diffusion into the Fin sidewall were also investigated for Fin conformal doping (14). As mentioned in ref 5 with diffusion doping from a solid source, maximum dopant activation will be limited to dopant solid solubility at a given temperature requiring very high annealing temperatures for high dopant activation but this can never achieve the very high activation level from an amorphous implanted junction using SPC. At 1000°C As monolayer deposition doping diffusion is limited to <5E20/cm^3 as reported by Duffy (15) and Kennel (5) due to As solid solubility limit in Si, in Ge at 650°C Duffy reports the same As monolayer doping activation is limited to only 6E18/cm^3.

20/22nm Node Application Processors

Intel's SoC 22nm Bulk-FinFET Doping and High Mobility Channel Strain-Si Technology for Windows Nokia & Low End China Smartphones

Intel introduced the 1st 3-D bulk-FinFET devices at 22nm node production in May 2012. The SoC process was used for low end China smartphone and Windows Nokia smartphone as described in their IEDM-2012 paper which states the FinFET process uses the overall process sequence from the 32nm planar SoC with the addition of Fin related diffusion (16). The Intel 32nm SoC process was reported at IEDM-2009 using 3 different S/D extension (SDE) implants for HP/LP logic, ULP and I/O with corresponding recess etch and refill p+ eSiGe S/D with 0nm overlap spacing for HP and SP, 5nm overlap spacing for LP and 12nm overlap spacing for I/O (17). The elemental analysis and strain channel level was reported by Ogura (18) to be 3.75GPa for PMOS and 850MPa for NMOS. Intel uses 8° tapered Fin sidewalls which allows for 45° high tilt angle SDE implantation for conformal doping. Ohmi reported the 8° taper results in the (551) crystal plane which is resistant to chemical etching surface roughening and optimized electron to hole mobility balance (19,20). James (21) of Chipworks reported the elemental analysis for the Fin structure at Semicon/West 2013 WCJUG seminar revealing P-S/D implants and As-SDE implants. This verifies the reported 45° amorphous As n+ SDE implant and deeper P n+ S/D implant reported by Rios (22) of Intel in 2011. Pipes (23) of Intel also reported and showed the partial Fin amorphization from the As SDE implant at 45° tilt that leaves Fins full of dislocation defect for NMOS stressor similar to the 32nm NMOS stressor. Highest retained implant dose and improved Fin sidewall line-edge-roughness (LER) on the atomic level can be realized with Hydrogen anneal for surface passivation as reported by Borland (24) especially for the lighter B and P implanted dopant atoms to keep the surface native oxide to <0.5nm. Highest dopant activation is achieved with msec annealing of amorphous implanted junctions by SPC and when C co-implant to suppress P S/D diffusion is combined with a deep amorphous structure, a boost in S/D stressor by 50% was observed (25). FinFET channel mobility enhancement at 22nm node used (551) plane tapered Fin with 55% eSiGe S/D compressive strain for PMOS with a very close gate to S/D overlap spacing of

-3nm and amorphous n+ As implant SPC with residual dislocation defect for NMOS S/D tensile stressor (16,21).

Localized within die and die to die 3-D FinFET transistor variability from SDE high tilt implantation with annealing now becomes more critical requiring tighter localized implantation tilted beam angle and dose control combined with uniform annealing techniques. Various implanter (as implanted) and annealing systems (near diffusion-less) non-uniformity signatures are shown in Fig.1 (26).

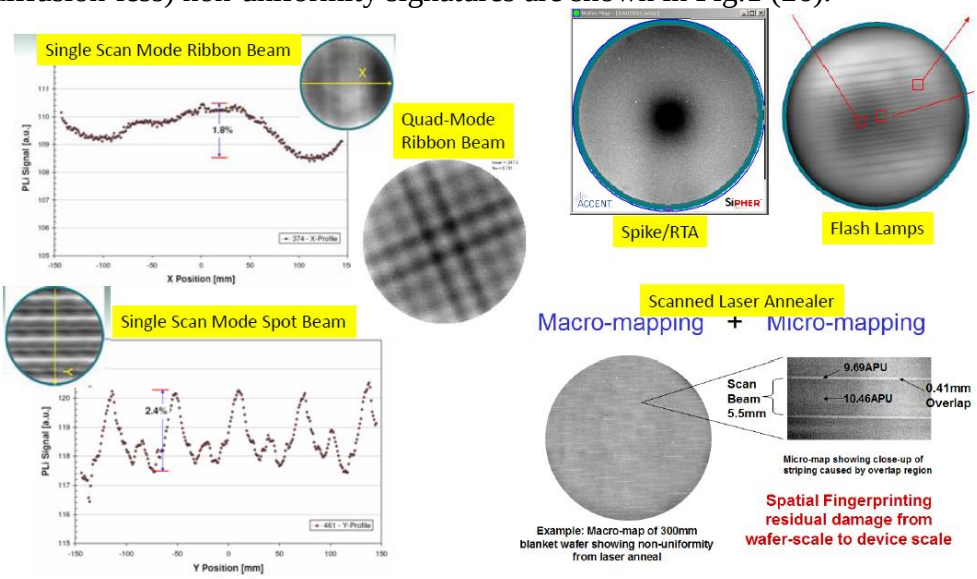


Fig.1: Unique non-uniformity signatures for various implanters and annealers.

<u>TSMC's 20nm Node 2-D Planar for Apple iPhone 6 A8 and Samsung Galaxy S5 Qualcomm Snapdragon Application Processors</u>

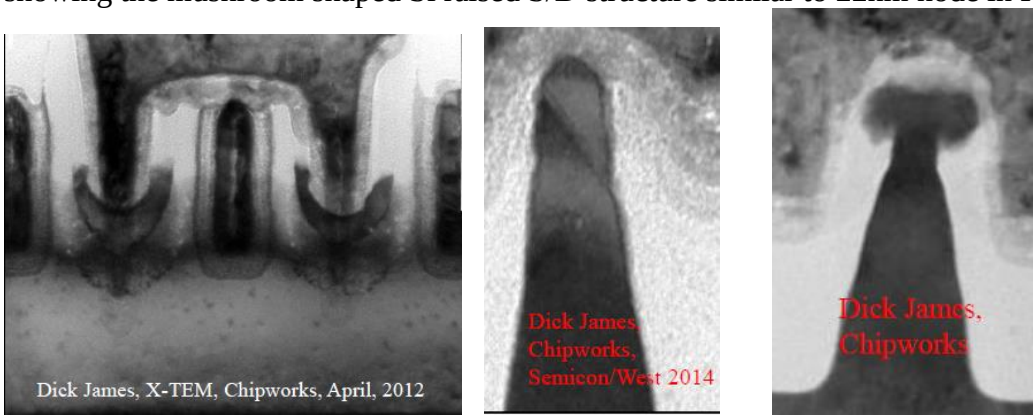
Both Apple A8 used in the iPhone 6 and Qualcomm Snapdragon application processor used in the Samsung Galaxy S5 uses TSMC's foundry 20nm 2-D planar technology. The PMOS uses eSiGe S/D compressive channel-strain similar to Intel's 32nm technology recess etch structure with a gate to S/D overlap spacing of 0nm while the NMOS uses a combination hybrid of Intel's 32nm amorphous implanted n+ S/D with SPC to create stacking fault dislocation defects for tensile channel-strain followed by partial recess etch embedded n+ raised S/D for improved contact resistance in the report by James of Chipworks (27) and TSMC's patent (28).

14/16nm Application Processor

<u>Intel's 14nm SoC Bulk-FinFET and High Mobility Channel Strain-Si Technology</u>

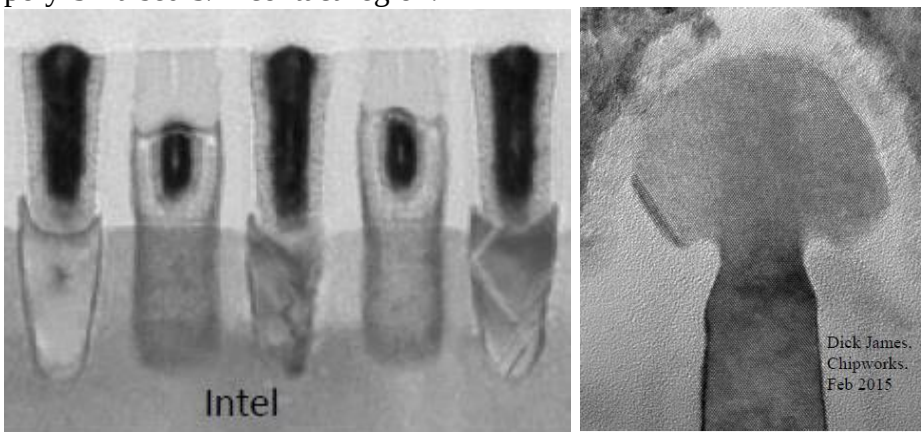
Intel introduced their 14nm 2nd generation bulk-FinFET technology in August 2014 and reported the details for the logic device at IEDM-2014 (29). The 14nm technology node uses taller vertical Fins without the (551) 8^{o} taper and kept the same SiGe content at 55% for the PMOS eSiGe S/D stressor but added a partial cavity recess etch embedded n+ raised S/D for NMOS with a large gate to S/D overlap spacing of 13nm. The Fin is full of dislocation defects resulting in a mushroom shaped raised S/D highly defective epi/poly structure suggesting they are using this stressor for tensile-channel strain since no end-of-range (EOR) defects can be seen in the SDE region compared to the 22nm node technology (Fig.2a and Fig.3a). Based on the Fin to Fin spacing I estimate they can still do up to 41^{o} high tilt extension implant in bi-mode or

>45^{o} tilt in quad-mode with 45^{o} wafer twist/orient for gate overlap control. They had to switch the sub-Fin doping from implant to spin-on-glass solid source diffusion due to the high aspect ratio Fin trench structure preventing the use of high tilt angle implantation doping of the Fin bottom region. The 14nm SoC technology was reported in June at VLSI Sym 2015 (30). X-TEM analysis for the 22nm N-FinFET by James of Chipworks is shown in Fig.2 with the well-defined n+ amorphous As-SDE residual implant damage after SPC anneal in Fig.2a along the NMOS Fin direction, Fig.2b through the SoC Fin S/D contact region with no raised S/D and Fig.2c logic region with a mushroom shaped poly-Si raised S/D. X-TEM analysis for the 14nm logic N-FinFET along the Fin direction from Intel's paper (29) is shown in Fig.3a showing no evidence of n+ SDE residual implant damage but clearly the n+ cavity etch and cavity refill with n+ raised S/D is full of epi/poly-Si dislocation defects. Fig.3b is from James of Chipworks showing the mushroom shaped Si raised S/D structure similar to 22nm node in Fig.2c.



a) b) c)

Fig.2: X-TEM of 22nm N-FinFET showing residual implant damage/dislocation defects a) along Fin direction, b) through the SoC Fin S/D contact region and c) logic Fin with poly-Si raised S/D contact region.



a) b)

Fig.3: X-TEM of 14nm N-FinFET showing a) along Fin direction of the n+ S/D cavity etch and dislocation epi refill and b) through the logic Fin with defective-Si raised S/D contact region.

Samsung's 14nm Bulk FinFET for Galaxy S6 and Apple iPhone 6s A9 Application Processor

Samsung introduced the Galaxy S6 in April 2015 using the Exynos 7 application processor with thier14nm node bulk-FinFET technology. No details on this process have yet been reported. However, Chipworks did report their teardown that Samsung's own

5Mp BSI is used for the front facing camera while Sony's 3-D stacked 16M pixel backside CMOS image sensor is used for the rear facing camera (31). Also the ePoP (package on package) consists of the 14nm Exynos AP, 28nm Qualcomm baseband processor, Samsung's 64Gb Flash memory and 3Gb LP DDR4 SDRAM. Looks like eSiGe S/D for PMOS stressor but not sure what is used for NMOS stressor.

TSMC's 16nm Bulk FinFET for Apple iPhone 6s A9 Application Processor

Waiting for Sept 2015 when Apple will introduce the next generation iPhone 6s with the A9 application processor with Samsung/foundry 14nm bulk-FinFET technology and TSMC's 16FF+ bulk-FinFET technology. At IEDM-2014 (32) the only information given in the TSMC paper is that it uses recess/raised S/D with dual epitaxy processing and this is TSMC's 2nd generation FinFET transistor (an enhanced 16nm CMOS technology). If like Intel they use the same process sequence ported over from the 20nm 2-D planar then it should also use high tilt SDE implants and n+ amorphous SPC dislocation defect stressor for NMOS S/D combined with the partial recess n+ S/D-epi. At VLSI Sym 2015 they reported on the 16nm FinFET SoC technology with multiple SDE implants for junction engineering to control SCE (short channel effect) and leakage but no images of the FinFET transistor in their presentation or paper (33). They said compared to logic the I/O transistor SDE implant is a graded lateral junction for lower leakage.

High Mobility SiGe or Ge Channel Material

7/10nm High Mobility Bulk or SOI FinFET Channels

At the 10nm or 7nm node localized higher mobility Fin/channel material is expected to be introduced. 50%-SiGe to 100%-Ge high mobility Fin-channel material on Si wafers will be realized by; 1) traditional gas/vapor phase epitaxial growth techniques using chemical vapor deposition (CVD) in blanket or selective growth including aspect ratio trapping or mesa etched defined regions/islands as reported by Mitard (34), 2) Ge condensation by localized oxidation of a lower Ge-content SiGe epilayer to form higher Ge-content Fin surface regions as reported by Hashemi (35) or 3) an alternative new method using dose controlled deposition (DCD) of an amorphous SiGe or Ge layer by high dose Ge-implantation followed by laser melt liquid phase crystallization (LPC) as reported by Borland (36-38).

Traditionally SiGe and Ge surface layers on bulk-Si or SOI wafers are realized by Chemical Vapor Deposition (CVD) epitaxial growth at elevated temperatures (400^{o}C to 800^{o}C) and Ge selective epitaxial growth (SEG) can be achieved with an oxide hard mask. To reduce misfits and threading dislocation defects at the epi/substrate interface strain relaxed buffer (SRB) or aspect ratio trapping (ART) have been employed with Ge-epi on bulk-Si while others have used Ge layer transfer wafer bonding techniques for GeOI or SiGeOI. One issue with Ge-epi growth by CVD is poor uniformity especially for thin layers 5-50nm and for selective epi it can be much worse due to pattern density local loading effects and nucleation delay time from surface impurities within the small oxide mask windows. Oxide sidewall induced defects can also degrade junction leakage and device performance requiring a mesa etch defined Fin structure for lowest junction leakage. Ion implantation has extremely tight uniformity of 0.2-0.5% and uses photoresist masking method so an alternative to Ge-epi by CVD is to use either SPC or LPC to form high quality single crystal Ge or SiGe epitaxial surface layers from an

amorphous 50-100% Ge deposited layer formed by DCD using the Si substrate wafer as a seed layer for single crystal epitaxial regrowth (36, 37). SPC annealing technique is commonly used with ion implantation when the implant dose is high enough to cause sufficient surface damage to amorphize it. Ge species is typically used to amorphize the surface region of Si when the dose is >5E14/cm^2 to depths from as shallow as 5nm (3keV) to 60nm (40keV) as reported by Borland for various implant species including Ge, Si, In, Sb and Xe, energies and doses (38).

Using high dose >E16/cm^2 Ge-infusion doping by Gas Cluster Ion Beam (GCIB) technique with photoresist soft mask was proposed in 2004 by Borland (36) resulting in localized amorphous Ge surface deposition 33-70nm thick by DCD with a reported uniformity of 0.52% on 300mm wafers. They reported using low temperature SPC to form single crystal Ge epitaxial layers but residual Ge implant end-of-range (EOR) damage remained beyond the amorphous crystalline interface. Using PR (photoresist) soft masking technique with high-k/metal gate last approach, localized high mobility Ge-channels could be formed by Ge doping directly into the channel region thereby leaving the n+ S/D regions composed of Si material for high n+ dopant activation, shallow junction formation avoiding enhanced diffusion of n-type dopant in Ge and therefore low n+ junction leakage (39). This proposal by Borland is shown in Fig.4 below. Today, the industry has moved from planar 2-D devices to 3-D FinFET devices requiring a change to the original proposal as shown in Fig. 4b where the Ge or SiGe Fin region is first formed then the n+S/D region is recess etched away and Si-SEG is selectively grown and then doped n+ by implantation leaving just Ge in the channel/Fin region. High n+ dopant activation in the n+Si S/D region is realized with minimal dopant diffusion similar to a Si-capping layer on Ge as reported by Borland & Konkola at IIT-2014 and reduced Ge-epi threading dislocation (40).

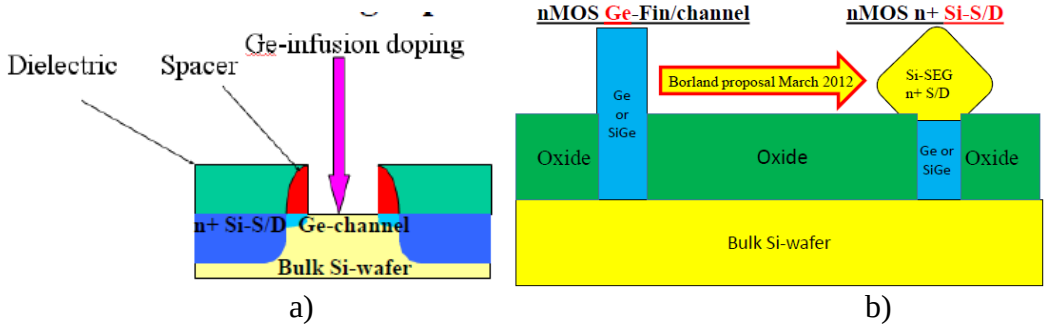


Fig.4: Formation of Ge-channel with n+ Si-S/D formation in 2-D planar or 3-D FinFET.

Laser melt annealing of implanted junctions are currently being used in production for high quality back-side illuminated CMOS image sensors used in smart phone cameras by several IC and foundry semiconductor manufacturers and if the melt depth exceeds the implant damage depth complete elimination of all residual implant damage/defects occurs with 100% dopant activation. At IWJT-2013 Borland (37) reported using Ge-plasma ion implantation at 1E16/cm^2 and 1E17/cm^2 doses with selective/localized laser melt annealing to realize high quality up to 55% Ge epilayer by LPC with >4x higher hole mobility (160cm^2/Vs) due to the high Ge surface level and surface strain without residual implant damage or EOR defects when the laser melt depth exceeded the amorphous Ge implant depth which was 60nm. One limitation they noted with plasma Ge implantation was poor retained Ge dose due to surface sputtering at low energies which limited the Ge content to 55% for the 1E17/cm^2 dose so 100% surface Ge by DCD could not be realized with plasma Ge implantation, 1E16/cm^2 Ge dose achieved

20% Ge. Therefore to overcome this retained dose problem they investigated Ge beam-line ion implantation to achieve higher retained dose for precise controlled Ge deposition by DCD at 5E16/cm^2 Ge implant dose which resulted in a 7.5nm thick a-Ge deposited surface layer and with low wavelength 248-532nm lasers for absorption depth 10-1000nm in Si (38). Borland reported on an alternative method using amorphous Sn implantation into the top 30nm of Ge-epilayers followed by LPC using laser melt annealing to form strain-Ge layers thereby improving electron mobility by 2x (41).

5nm Exploratory Research Si or Ge Nano-wire Gate-All-Around (GAA) Devices

At 5nm node Si, SiGe or Ge nano-wire gate-all-around devices will be implemented. Horizontal or lateral nano-wire (NW) fabrication seems simplest compared to vertical nano-wire especially if using the multiple layer deposition, etch and lateral undercut removal methods. These include using SOI, SGOI, GOI or bulk Ge/Si wafers. At IEDM-2013 Hur (42) showed a simple way for Si-NW fabrication. Using multiple layers of Si/SiGe/Si/SiGe/Si epilayers you trench etch the bulk Fin structure followed by selective SiGe wet etching to leave a suspended stacked Si-NWs. GeSn-NW can be formed by growing stacked Ge/GeSn epilayers followed by Fin trench etching and selective Ge wet etch (43). High temperature Hydrogen annealing results in the transformation of rectangular Ge-NW to circular Ge-NW (44).

Another option at 5nm node is to go to 3-D VLSI by stacking transistors at the gate level as proposed by CEA LETI called "CoolCube" (45-47). They reported the bottom FET can be processed at high Si temperatures >1000^{o}C but the top FET must be low temperature <600^{o}C RTA or <700^{o}C nsec laser annealing (46). The top FET can also be Ge for low temperature processing and better dopant activation and will require extension implants 1st (X^{1st}) rather than extension implant last (X^{last}) for best gate overlap control and >25^o tilt amorphous X^{1st} implant followed by SPC for highest dopant activation (47).

High Dopant Activation and Low Leakage n+ USJ in Ge and SiGe Material

Embedding Si-CMOS technology with localized regions of 50-100% Ge material for high mobility channels will start to occur at the 10nm node and beyond for both pMOS and nMOS devices. The historical dopant solid solubility limit comparative data for Si and Ge was reported by Trumbore (48) dating back to 1959 is missing data for B and P in Ge and only shows solid solubility data for p-type Ga dopant starting at 24^{o}C (room temperature) and n-type As starting at 750^{o}C with Sb starting at 600^{o}C. Implant damage in Ge material creates acceptor defect levels as high as 7E19/cm^3 (40) requiring annealing temperatures >600^{o}C to eliminate them for stable p+ or n+ junctions in Ge as reported by Zaima (49). This could explain why many have reported excellent implanted p-type B dopant activation in Ge at very low temperatures and difficulties with n-type dopant activation requiring dopant compensation.

USJ n+ Junctions in Ge Material

One major issue for Ge NMOS is the difficulty in achieving both n+ ultra-shallow junction (USJ) and high dopant activation. Implanted P, As and Sb n+ dopant activation in Ge using traditional RTA annealing increases with temperature as reported by Borland and Konkola (40) reaching saturation above 875^{o}C. To prevent rapid diffusion of n+ dopant in Ge and achieve USJ, the RTA annealing temperature must be kept below

600ºC but this reduces dopant activation level by 70% to low-E19/cm^3 as reported by Lee (50). The best n+ dopant activation is right at the melting point of Ge at 937ºC and rapid n+ liquid phase diffusion to the liquid/solid interface occurs so the n+ junction depth is determined by the Ge layer thickness. As the temperature exceeds 937ºC, Si intermixing occurs forming a SiGe alloy degrading both mobility and n+ dopant activation level. The solution is to use rapid and controlled Ge melt depth without Si intermixing to define the n+ junction depth in Ge. An example of melt depth controlled n+ junction in Ge using laser melt annealing was reported by Mazzocchi (51) achieving P dopant activation level >1E20/cm^3. Thareja (52) reported higher n+ activation for Sb compared to P and As using laser melt to control junction depth and defects for low leakage achieving Sb activation up to 4E20/cm^3 with As and P both at 2E20/cm^3. Using a 308nm laser Borland (41) reported Sb implanted n+ junctions in Ge with Xj <10nm and >1E21/cm^3 dopant activation. Adding Sn co-implants increased electron mobility by 2x to 144cm^2/V-s. Also at annealing temperatures above 600ºC, care must be taken to minimize and prevent both Ge and/or dopant surface loss if not using a surface capping layer.

Ge n+ junction leakage is also more sensitive than in Si, higher annealing temperatures and deeper n+ junctions usually results in higher junction leakage. Lee (53) reported higher temperature RTA annealing at >600ºC results in higher n+ Ge junction leakage current and this effect is reduced with oxygen co-implantation. They did not observe this effect with p+ Ge junctions and they used Ge-Cz bulk wafers. Shayesteh (54) also compared 500ºC RTA to laser melt annealing for P n+ junction leakage in Ge and reported deeper junction depth (laser melt depth) to 80nm reduced junction leakage by 100x, however, RTA n+ junction leakage was still 100x better with junction depth of 120nm and P surface dopant level of <1E19/cm^3 compared to laser at >7E19/cm^3.

Summary

Starting this year (2015) smartphones will included both More-Moore scaling with 14/16nm 3-D FinFET application processors used in Samsung Galaxy S6 and Apple iPhone 6s as well as More-than-Moore with Sony's 3-D stacked back-side CMOS image sensors and Samsung's ePoP with 3-D stacked chips. Next for 10nm and 7nm node will be higher channel mobility material with 50%-SiGe to 100%-Ge and at 5nm Si, SiGe or Ge nano-wire devices or 3-D gate stacked VLSI like the CoolCube. 3-D FinFET doping will continue to use tilted beam-line X^{1st} implantation for the critical SoC/AP gate overlap control. Best Ge n+ dopant activation of >1E21/cm^3 is realized with Sb and laser melt LPC to control sub-10nm Xj. Sn co-implant improved electron mobility by 2x and Ge DCD for localized 50%-SiGe to 100% Ge channel formation by LPC.

References

1. J. Borland et al., Solid State Technology, June 2003, page 52.
2. R. Duffy et al., Insights 2007, p.241.
3. J. Mody et al., IWJT-2011, paper S8-2, p. 108.
4. J. Borland et al., Insights 2009, p.352.
5. H. Kennel et al., IEEE RTP-2006, p.85.
6. S. Beismen, Semicon West 2011 presentation material.
7. J. Borland et al., IEEE-RTP 2010, p.18.

8. H. Onoda et al., IWJT 2013, paper S6-1, p.66.
9. M. Togo et al., VLSI Sym 2013, paper 14-2, p. 196.
10. A. Kambham et al., VLSI Sym 2012, paper 9.1.
11. S. Felch et al., IWJT-2011, paper S2-1.
12. G. Fuse et al., SSDM 2010, paper P-1-23-L.
13. Y. Sasaki et al., IEDM 2013, paper 20.6.
14. K. Ang et al., IEDM 2011, paper 35.5.
15. R. Duffy et al., IWJT 2014, paper S7-05.
16. C. Jan et al., IEDM 2012, paper 3.1
17. C. Jan et al., IEDM 2009, paper 28.1.
18. Prof A. Ogura of Meiji University private presentation material, July 2012, SSDM 2011, paper E-7-3, p.933 and ECS Oct 2014 paper P7-1765.
19. T. Ohmi et al., IEEE Trans on Electron Devices, vol.54, no.6, June 2007.
20. R. Kuroda et al., SSDM 2013, paper D-1-5, p.702.
21. D. James, Chipworks teardown of Intel 22nm FinFET, Semicon West 2013, AVS-WCJUG seminar material.
22. R. Rios et al., IEEE EDL, vol.32, no.9, Sept. 2011.
23. L. Pipes et al., IIT 2014, p.37.
24. J. Borland et al., IWJT 2011, paper S7-3.
25. J. Borland et al., IEEE-RTP-2009, paper 7, p.59.
26. J. Borland et al., IWJT 2007, paper S3-3, p.39.
27. D. James of Chipworks tear down of TSMC's 20nm, Oct. 2014.
28. TSMC's 20nm US Patent #8,674,453 B2, March 18, 2014.
29. S. Natarajan et al., IEDM 2014, paper 3.7.
30. C. Jan et al., VLSI Sym 2015, paper 2-1.
31. D. James, Chipworks blog on Samsung Galaxy S6 smartphone, April 6, 2015.
32. S. Wu et al., IEDM 2014, paper 3.1.
33. T. Miyashita et al., VLSI Sym 2015, paper 11-3.
34. J. Mitard et al., VLSI Sym 2014, paper 13.2.
35. P. Hashemi et al., VLSI Sym 2015, paper 2.3.
36. J. Borland et al., ECS Oct 2004, PV2004-07, p.769.
37. J. Borland et al., IWJT 2013, paper S4-4, p.49.
38. J. Borland et al., ECS Oct 2014, paper P7-1771.
39. J. Borland et al., Solid State Technology July 2005, p.45 and US Patent #7,259,036.
40. J. Borland & P. Konkola, IIT-2014, p.43.
41. J. Borland et al., IWJT 2015, paper S2-1, p.12.
42. S. Hur et al., IEDM 2013, paper 26.5.
43. X. Gong et al., VLSI Sym 2013, paper 3-5.
44. J. Hoyt, ECS Oct 2011, presentation material.
45. C. Fenouillet-Beranger et al., IEDM 2014, paper 27.5.
46. P. Batude et al., VLSI Sym 2015, paper 5-2.
47. L. Pasini et al., VLSI Sym 2015, paper 5-3.
48. F. Trumbore, ECS May 1959 Philadelphia meeting, p.205.
49. S. Zaima et al., ECS Oct 2014, paper P7-1772.
50. Y. Lee et al., IEDM 2012, paper 23.3, p.513.
51. V. Mazzocchi et al., IEEE-RTP 2009, paper 21.
52. G. Thareja et al., IEDM 2010, paper 10.5, p.245.
53. C. Lee et al., IEDM 2014, paper 32.5.
54. M. Shayesteh et al., IEEE Trans. on Elec. Devices, vol.61, no.12, Dec 2014, p. 4047.