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Smartphone Market Driving 7nm & 5nm Node 3-D Devices and Stacked Devices

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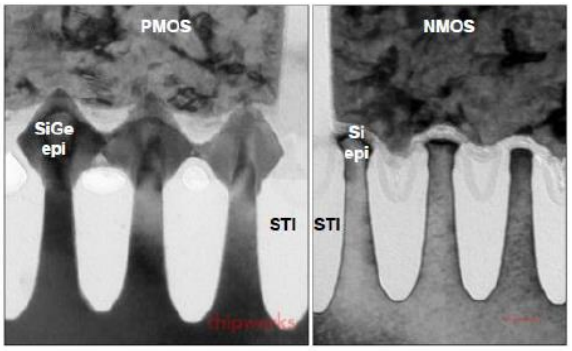
Abstract

Advanced Logic devices continue with More Moore device scaling with the switch to 3-D transistor architectures going from 2-D planar to 3-D FinFET at 22nm node by Intel in 2012 and at 14/16nm node in 2015 for smartphone application processor used in Samsung Galaxy S6/edge and Apple iPhone 6s/plus. FinFET will be replaced with 3-D stacked Gate-All-Around (GAA) Nanowire or Monolithic 3-D stacked 2-D planar transistors at sub-5nm node. More than Moore 3-D stacked devices in a single package was introduced by Sony in Jan 2012 for backside CMOS image sensor and used by Apple in iPhone 5s/5c with the pixel array stacked over logic using through silicon via (TSV). Then in April 2015 Samsung introduced in the Galaxy S6/edge embedded package on package (ePoP) by stacking the DRAM memory and NAND Flash memory in a single memory package and position this directly on top of the application processor saving 40% area and allowing for compact form factor needed to keep smartphones (mini mobile computers) in a small handheld device.

Introduction

In 2015 the worldwide IC market was $333B with about 30% going into the 1.43B smartphone market, up 13.5% from 2014 compared to <24% ICs going into the declining PC/tablet market as smartphones become the mini mobile computers in capabilities and the central hub/gateway for the Internet of Things (IoT) devices including wearables and home monitoring devices. Samsung Galaxy smartphone is #1 with worldwide market share at 22.4% followed by #2 Apple iPhone at 11.8%. Since 2011 the high end smartphone application processor (AP) has advanced a logic technology node every year. The Apple A5 in the iPhone 4s in 2011 used 45nm node, in 2012 the iPhone 5 A6 used 32nm node from Samsung, in 2013 iPhone 5s/5c A7 used 28nm node from Samsung, in 2014 iPhone 6/plus A8 used 20nm node from TSMC and in 2015 iPhone 6s/plus A9 used 14nm node from Samsung and the 16nm node from TSMC. The next generation AP from Apple for iPhone 7/plus will be the A10 using the current 16nm node from TSMC since the 10nm node will not be ready until 2017 for the A11. Fig.1 shows the 16nm FF+ from TSMC used for the A9 in iPhone 6s/plus and Fig.2 shows the 14nm node FinFET from Samsung used for the A9 in iPhone 6s [1]. The Samsung Galaxy S4 in 2013 used 28nm node for AP, the Galaxy S5 in 2014 used Qualcomm's Snapdragon AP with 20nm node from TSMC, the Galaxy S6/edge in 2015 used the Samsung internal AP Exynos with 14nm node from Samsung and the Galaxy S7/edge in 2016 used the Qualcomm Snapdragon AP with 14nm node from Samsung. Next year in March 2017 the Galaxy S8 AP is expected to use the 10nm node from Samsung. So today the smartphone AP is

driving More-Moore continued device scaling and not driven by the PC microprocessor anymore. More than Moore 3-D stacked technologies are also being driven by the smartphone market. In Jan. 2012 Sony introduced the first stacked backside CMOS image sensor with the pixel array on top of the logic circuit using TSV (through silicon via) shown in Fig.3 [2]. The iPhone 5 in 2012 incorporated the Sony 8Mpixel stacked backside CMOS image sensor for rear facing camera. The next More than Moore 3-D stacked technology to be incorporated into smartphones was by Samsung when in Feb 2015 they introduced the extremely thin ePoP (embedded package on package) memory, a single memory package consisting of 3GB LPDDR3 DRAM and 32GB NAND Flash that's then positioned on top of the application processor rather than beside it decreasing the total area used by approximately 40%. This was first used in the Galaxy S6/edge smartphones beginning in April 2015. Also in 2015 Samsung's 128Gb Flash memory was offered as either 2-D planar using 16nm technology or 3-D 32-layer stack using 40nm technology as shown in Fig.4 [1]. In March 2016 Samsung introduced the Galaxy S7 with an optional microSD card with up to 256Gb Flash memory then in August 2016 Samsung announced their 512Gb Flash memory chip using 64-layers.



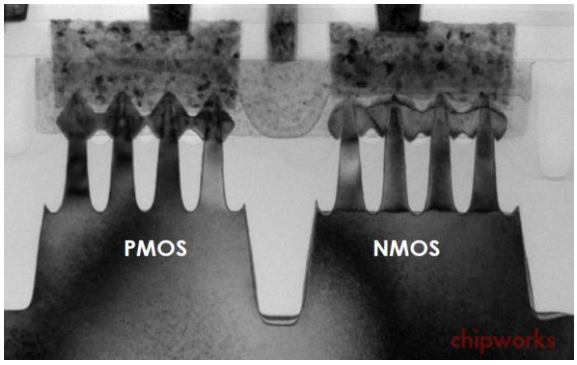
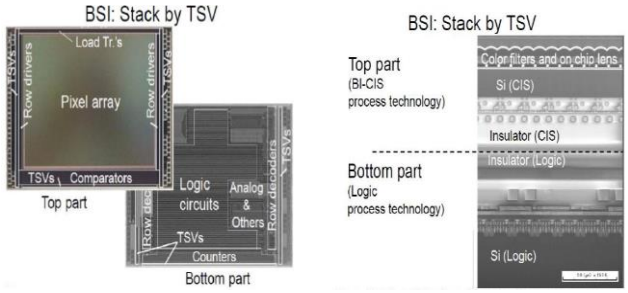


Fig.1. TSMC 16nm FF+ for A9 iPhone-6splus [1].**Fig.2**. Samsung 14nm FinFET for A9 iPhone-6s[1].



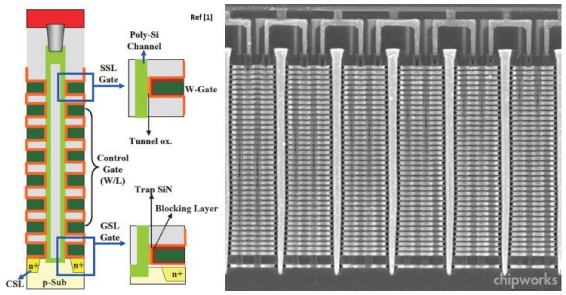


Fig.3. Sony's 8Mp stacked backside CIS [2]. **Fig.4.** Samsung 128Gb 3-D Flash with 32-layers 40nm node [1].

3-D Bulk FinFET Transistor Formation

Intel was first to introduce 3-D bulk FinFET at the 22nm node in 2012. Fig.5 shows the X-TEM cross-section through the Fin S/D contact region showing the (511) 8^{o} taper 8nm wide Fin. Fig.6 shows the X-TEM along the Fin direction revealing the n+S/D with residual implant damage and 55% eSiGe p+S/D with -3nm recess etch under the gate edge for S/D-stressor. Chemical analysis of the n+S/D Fin region by Ogura of Meiji University is shown in Fig. 7, the As extension implantation in Green, the P S/D implantation in Orange and the C S/D-stressor implantation in Red [3]. For 14nm node Intel's Fins are taller, vertical with n+ S/D Si-epi [4].

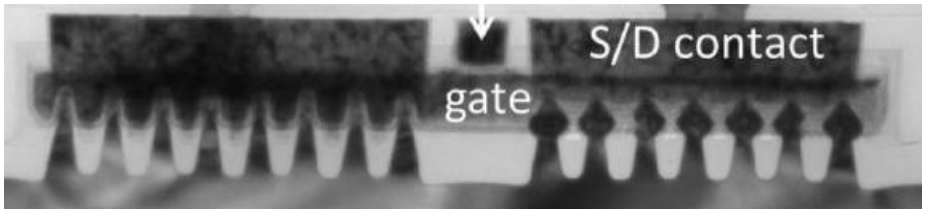


Fig.5. Intel's 22nm FinFET X-TEM through the Fins showing n+S/D and eSiGe raised p+S/D [1].

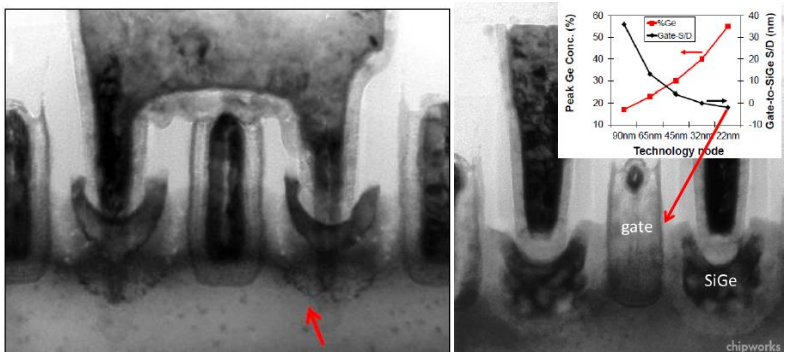


Fig.6. Intel's 22nm FinFET X-TEM along the Fin direction showing n+S/D and eSiGe raised p+S/D [1].

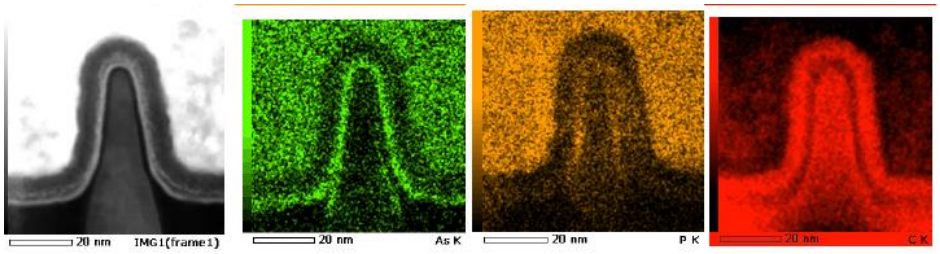


Fig.7. Chemical analysis of nMOS transistor showing As-SDE, P-S/D and C-S/D implants [3].

3-D Gate-All-Around Nanowire Transistor Formation for sub-5nm node or Monolithic 3-D stacking

At sub-5nm node the industry will switch from FinFET to lateral GAA nanowires that can be stacked above each other based on the number of multiple Si/SiGe/Si/SiGe stacked epilayers as shown in Figs.8 & 9 to form Si-nanowires or Ge/GeSn/Ge/GeSn stacked epilayers for Ge-nanowire formation [5-7]. After the vertical etching the Fin, SiGe or GeSn material can be selectively etched away leaving free standing rectangular shaped rods of Si or Ge that when annealed in hydrogen ambient becomes round and cylindrical forming the nanowire. Another option at sub-5nm node is to go vertical similar to 3-D Flash and stack multiple layers of 2-D planar transistors using multiple layer transfer bonded-SOI technology. This allows the end for logic device More-Moore scaling by increasing transistor density with vertical stacking as reported by LETI 's "CoolCube".

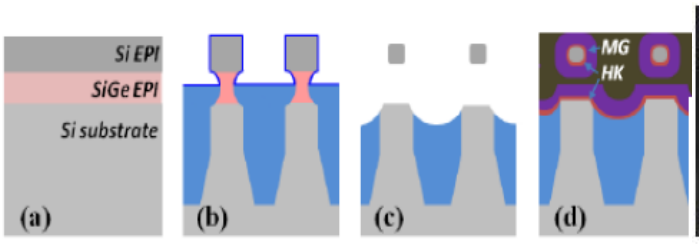


Fig.8. Horizontal GAA nanowire formation [5].

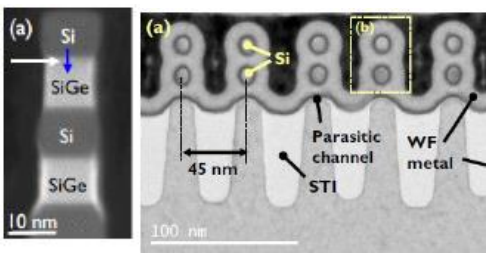


Fig.9. Stacked GAA nanowire [6].

3-D FinFET High Mobility Channel Formation

Intel introduced higher mobility channels starting at the 90nm node back in 2003 using eSiGe for p+S/D-stressor. As shown in Fig.10 the Ge content was increased for each technology node from 17% at 90nm node to 55% for 22nm & 14nm node. At the same time the S/D recess etch under the sidewall spacer/gate edge went from +35nm to -3nm. At 55% Ge the compressive channel strain of -3GPa has reached saturation limit for a hole mobility of 400cm^2/V-s as shown in Fig.11 therefore higher mobility channel material is needed for 10nm node and beyond such as tensile or compressive strain-Ge or strain-SiGe. Borland reported localized tensile and compressive strain Ge formation using Sn, Ge, C or Si implantation with advanced annealing [8]. Fig.12 shows the results for Sn implantation into Ge to create localized tensile strain as shown by the XRD Ge peak hump to the left and measured improved electron mobility by 2.5x going from 500cm^2/V-s to 1400cm^2/V-s.

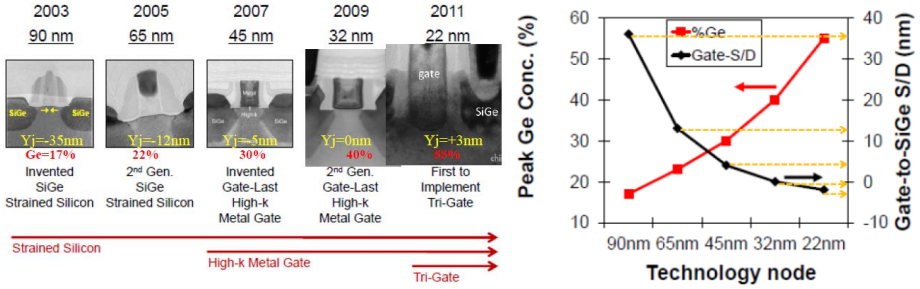


Fig.10. Evolution of Intel's eSiGe p+S/D-stressor.

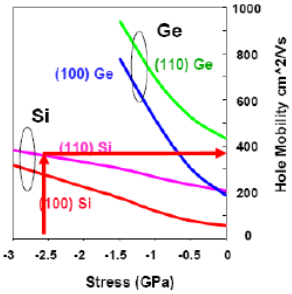


Fig.11. Compressive strain effects on μ_h.

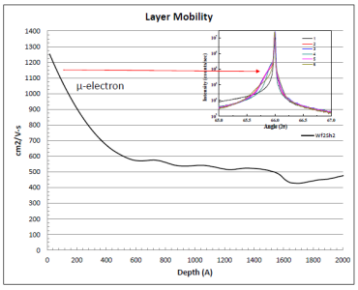


Fig.12. Sn-implant effects on Ge μ_e [9].

Summary

Smartphone ICs are driving the semiconductor industry to More-Moore device scaling and More than Moore 3-D stacked technologies with nearly 1.5B units a year out numbering PC/tablets by nearly 5x. The application processor currently uses 14/16nm node 3-D bulk FinFET transistors, the microSD card can be 3-D Flash memory with 32, 48 or 64 layers, the rear facing camera is 12-16Mpixel 3-D stacked backside CIS and 3-D stacked ePoP.

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