High Electron and Hole Mobility By Localized Tensile & Compressive Strain Formation Using Ion Implantation and Advanced Annealing of Group IV Materials (Si+C, Si+Ge & Ge+Sn)

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This paper will review strain-Si and strain-Ge formation by ion implantation and advanced annealing to form localized tensile and compressive strain channel for improved electron and hole mobility in Group IV materials. Carbon implant was used to reduce the surface Si lattice constant forming Si+C material for localized compressive strain-Si channel. Ge implant was used to increase the surface Si lattice constant forming Si+Ge material for localized tensile strain-Si channel and Sn implant to increase the surface Ge lattice constant forming Ge+Sn material for localized tensile strain-Ge channel. Use of ion implant and advanced annealing for strain formation resulted in tensile strain-Si+Ge improving hole mobility by 4x and electron mobility by 1.5x while tensile strain-Ge+Sn improved electron mobility by 2-2.5x.

Introduction

Since the introduction of the 90nm node in 2003 by Intel the industry has been using recess etched eSiGe-epi p+S/D-stressor to induce up to -3GPa compressive channel strain-Si for increased PMOS hole mobility (μ_h) by 2-5x while they used other techniques to induce tensile channel strain for increased NMOS electron mobility (μ_e) including CVD tensile stress liner (1). In 2007 at the VLSI Sym Wei et al of AMD reported eSiGe p+S/D stressor for PMOS at the 65nm node N3 and for the N5 use of implanted n+S/D-stressor by gate edge stacking fault dislocation formation they called SMT (stress memorization technique) by using an amorphous S/D implantation to induce tensile channel strain-Si increasing μ_e and 10% higher drive current for PD-SOI (2). In 2008 Rudawski et al from the University of Florida had a more detailed paper reporting deep amrophous implant with SPE crystallization anneal to create mask edge stacking fault dislocation that results in compressive strain-Si in the amorphous S/D region after Solid Phase Epi-Crystallization (SPEC) and tensile strain-Si in the non-implanted channel region (3). Also in 2007 at VLSI Sym, Liu et al of IBM reported carbon implantation to form 1.65% Si+C as an alternative to eSiC-epi for NMOS n+S/D-stressor to induce up to 600MPa tensile channel strain-Si resulting in a 6% higher drive current for the 65nm node PD-SOI (4). But it was not until 3 nodes later, the 22nm node PD-SOI technology in 2012 that IBM introduced 1.5% SiC into production using eSiCP-epi n+S/D stressor which induced 340MPa tensile channel strain-Si (5). The key to successful S/D stressor implementation is optimizing the deep S/D with the shallow SDE implant junction for high dopant activation, low junction leakage and minimal strain relaxation annealing effects. From the periodic table the key group IV elements used in silicon semiconductor processing have the following lattice constant: C=3.56Å, Si=5.43Å, Ge=5.64Å and

Sn=6.48Å as shown in Fig.1. The effects on changing the crystal lattice spacing from the reference Si results in multiple XRD peaks to the right of the main Si-peak for SiC due to smaller C lattice and compressive strain and multiple peaks to the left of the main Si-peak due to larger Ge lattice and tensile strain-Si. GeSn epi peak is to the left of the main Ge peak due to tensile strain-Ge formation. Based on the lattice constant in Fig.1 10% Sn would increase Ge lattice constant by 1.3% and 3% C would decrease Si lattice constant by 1.0%.

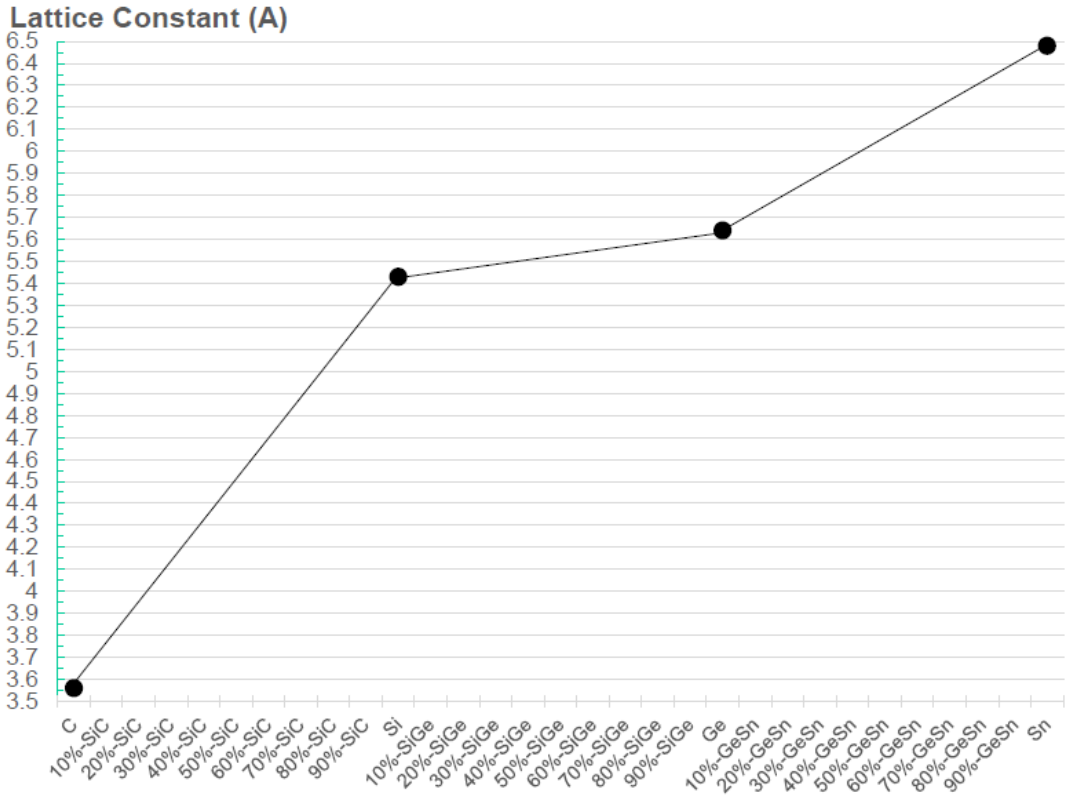


Fig.1: Lattice constant for C, Si, Ge and Sn.

PMOS S/D Stressor evolution from 90nm to 14nm node

The evolution of the PMOS eSiGe S/D stressor has been well documented by Intel in their numerous publications as shown in Fig.2: 1) 90nm node in 2003 used 17% SiGe with gate to S/D spacing of 35nm creating -300MPa channel strain and improved μ_h by 1.5x from 65cm^2/Vsec to 100cm^2/Vsec, 2) 65nm node in 2005 used 22% SiGe with gate to S/D spacing of 12nm creating -900MPa channel strain and improved μ_h by 2.7x to 180cm^2/Vsec, 3) 45nm node in 2007 used 30% SiGe sigma-shaped with gate to S/D spacing of 5nm creating -1.5GPa channel strain and improved μ_h by 3.8x to 250cm^2/Vsec, 4) 32nm node in 2009 used 40% SiGe with gate to S/D spacing of 0nm creating -2.2GPa channel strain and improved μ_h by 4.6x to 300cm^2/Vsec, 5) 22nm node FinFET in 2011 used 55% SiGe with gate to S/D spacing of -3nm creating -2.5GPa channel strain and improved μ_h by 5.1x to 330cm^2/Vsec and 6) 14nm node FinFET in 2014 kept SiGe at 55% due to saturation of channel strain at -2.5GPa and μ_h at 330cm^2/Vsec (6). Therefore direct higher mobility channel material is needed for PMOS at sub-10nm node such as strain-SiGe or strain-Ge.

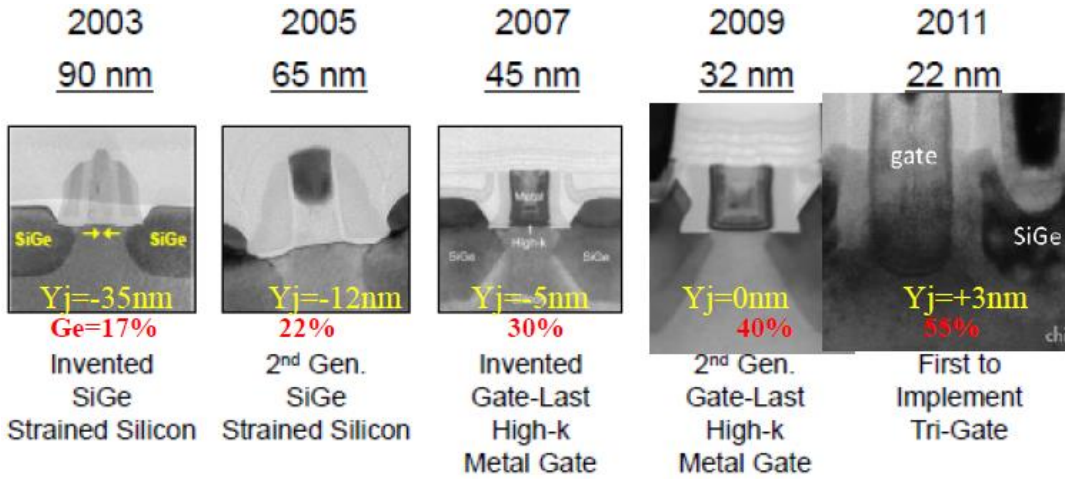
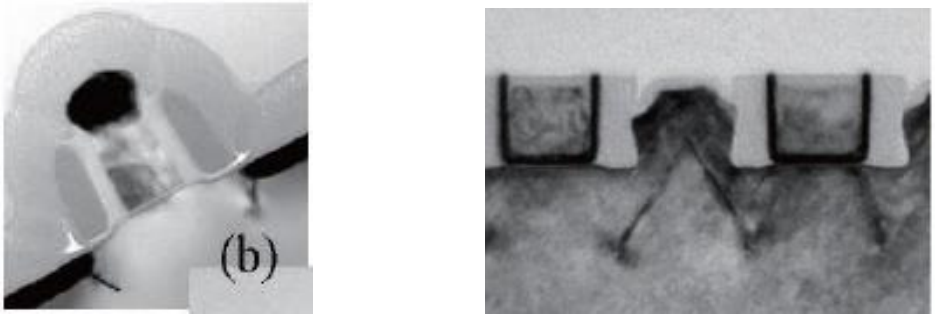


Fig.2: Intel eSiGe p+ S/D stressor fron 90nm node to 22nm node.

NMOS S/D Stressor Evolution from 65nm to 14nm nodes

Very little data on the evolution of the NMOS eS/D stressor can be found in the literature compared to the PMOS eSiGe S/D stressor. The 1st reported used of NMOS S/D stressor was by AMD at the 65nm N5 PD-SOI node using an amorphous implant for S/D compressive strain forming gate edge stacking fault defect in Fig.3 that induces channel tensile strain-Si for increased μ_e with 10% increase in drive current (2).



a) b)

Fig.3: Gate edge n+S/D stacking fault defect stressor a) AMD 65nm node PD-SOI and b) IBM Alliance 22nm node HK/MG-last bulk-CMOS gate edge n+ S/D stacking fault stressor.

For the 45nm node use of tensile stress liner for NMOS was standard but at the 32nm node in 2009 Intel also implemented the amorphous S/D implant gate edge stacking fault defect stressor using a high dose Si implantation for amorphization in Si and SiC S/D material as described in their US patent app #2010/0038685A1 (7). No process details were given by Intel except dislocation stress up to 650MPa and 20% drive current gain mentioned in their patent, however, Meiji Univ analysis of the Intel 32nm chip at SSDM 2010 reported this created 850MPa n-channel tensile strain-Si by the n+S/D gate edge stacking fault dislocation stressor while the eSiGe p+S/D stressor created -3.75GPa p-channel compressive strain-Si (8). The Raman Si-peak shoulder-hump to the left for tensile channel strain-Si and to the right for compressive channel strain-Si is shown in Fig.4. At the 22nm node in 2011 Intel switched to 3-D FinFET designed and the EDAX chemical analysis by Meiji University shows high levels of C in the n+S/D region forming eSiC stressor. Intel also reported the n+S/D-Fin after implant

is amorphous which will further boost the implanted Si+C S/D stressor by 50% as reported by Borland et al. (9).

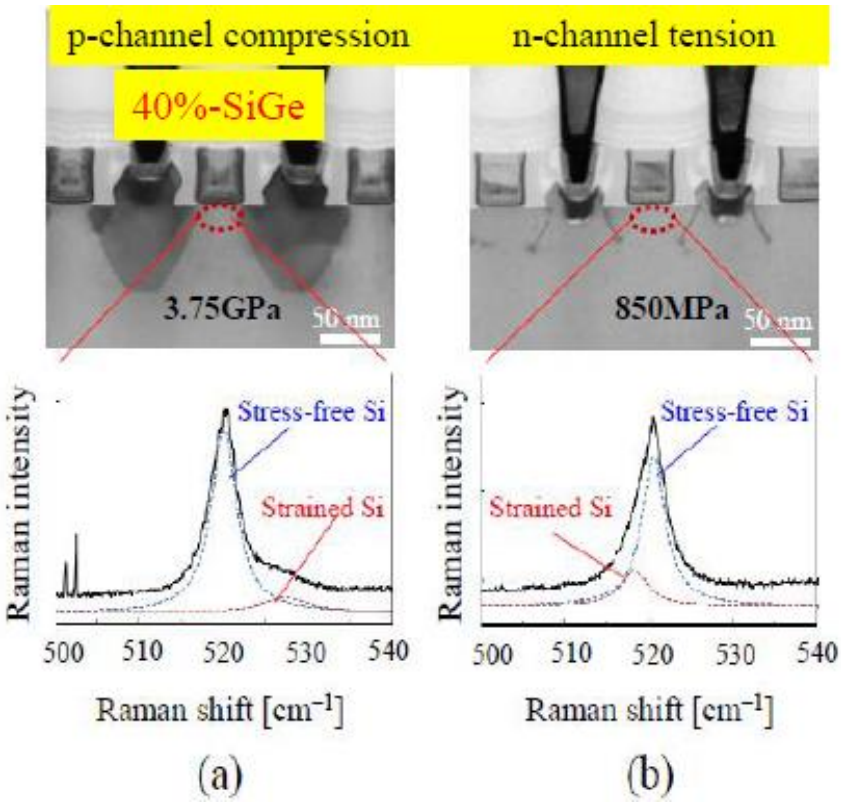


Fig.4: X-TEM and Raman of Intel 32nm node S/D stressors by a) eSiGe epi for pMOS and b) gate edge stacking fault defect by amorphous S/D implant for nMOS.

At IEDM-2012 IBM reported 22nm PD-SOI HK/MG-first will use 1.5% eSiC-epi for n+ S/D compressive stressor to create 340MPa n-channel tensile strain-Si and this was used in IBM Power 8 server processor (5). Then at the 2013 VLSI Sym IBM reported their 20nm bulk CMOS HK/MG-last will use the gate edge stacking fault dislocation n+S/D stressor similar to the SMT process from AMD 65nm node (10). TSMC's 20nm node technology for the Qualcomm Snapdragon used in the Samsung Galaxy-S5 smartphone and Apple A8 iPhone 6 used n+ S/D stressor that combines deep amorphous implant for gate edge stacking fault dislocation S/D stressor formation with a shallow recess etch eSiP-epi as reported in US patent #8,674,453 B2 to induce tensile n-channel strain-Si (11).

PMOS strain-Si S/D-stressor for higher p-channel μ_h has reached its limit at 14nm node requiring direct higher mobility channel material at 10nm and beyond by using: 1) relaxed >70% SiGe to 100% Ge or 2) compressive strain >50% SiGe to 100% Ge for higher hole mobility (12). Higher n-channel μ_e requires: 1) relaxed >95% SiGe to 100% Ge, 2) tensile strain-Si on >25% relaxed-SiGe or 3) tensile strain >50% SiGe to 100% Ge. Using CVD epitaxial growth of SiGe and Ge requires thick SRB (strain relaxed buffer) epilayers by blanket or selective epitaxial growth but this results in threading dislocation density (TDD) in the 10^6 to $10^9/cm^2$ level degrading n+ and p+ junction leakage as reported by Simoen et al of IMEC (13). The reported targets for NMOS is 2% tensile channel strain of >1.5GPa while for PMOS, 2% compressive channel strain of >-1.5GPa

at 7nm node as reported by Kim of Intel at IEDM-2015 is shown in Fig.5 (14). Therefore, this paper will review strain-Si and strain-Ge formation by ion implantation and advanced annealing to form localized tensile and compressive channel strain for improved μ_e and μ_h in Group IV materials by Ge, Sn and C implantation.

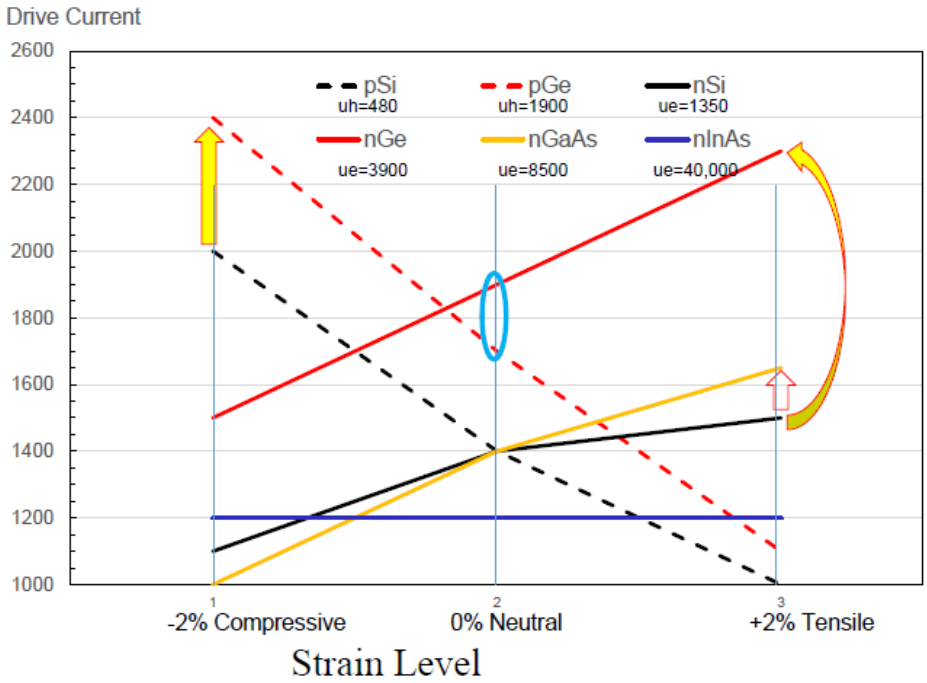


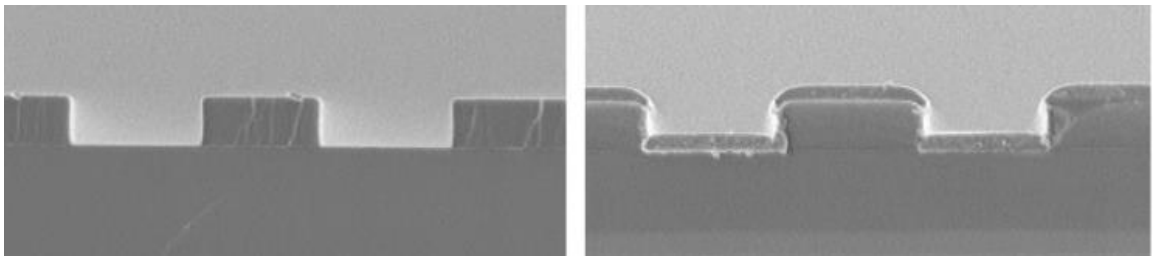
Fig.5: Strain level requirements for improved drive current at 7nm node.

Strain-Channel Formation by Ion Implantation

Si+Ge & Ge Channel Formation by High Dose Ge Implantation >5E16/cm^2:

An alternative to Ge-epi by CVD is to use either SPEC (solid phase epi-crystallization) or LPEC (liquid phase epi-crystallization) to form high quality single crystal Ge or SiGe surface layers from an amorphous Ge (a-Ge) layer using the Si substrate wafer as a seed layer for single crystal epitaxial regrowth/crystallization. SPEC annealing technique is commonly used with ion implantation when the implant dose is high enough to cause sufficient surface damage to amorphize it. Ge species is typically used to amorphize the surface region of Si when the dose is >5E14/cm^2 to depths from as shallow as 5nm at 3keV to 60nm at 40keV. When the Ge dose is 100x higher, a-Ge deposition occurs called dose controlled deposition (DCD). At 5E16/cm^2 dose a-Ge is ~7.5nm thick and at 4E17/cm^2 dose a-Ge is ~90nm thick. Borland et al. at the Oct 2004 ECS meeting reported localized a-Ge deposition 33-200nm thick by DCD using a photoresist soft mask as shown in Fig.6 with deposition uniformity of 0.52% on 300mm wafers with details reported in Epion/TEL US Patent #7,259,036 B2 (15, 16). They used low temperature SPEC to form single crystal Ge layers but residual Ge implant end-of-range (EOR) damage from the Gas Cluster Ion Beam (GCIB) method remained beyond the amorphous crystalline interface shown in Fig.7. Raman analysis for strain-Si is shown in Fig.8 with a shoulder/bump to the left of the main Si peak for the 950^{o}C anneal due to tensile strain-Si formation. They also observed that the Si surface native oxide can degrade the crystallization of the a-Ge deposited layer so Fig.9 shows the SIMS interfacial oxide areal density for a 12nm a-Ge DCD with and without an HF Si surface

clean. HF cleaning reduced the interfacial O areal density by two orders of magnitude from 2E15/cm^2 to 4E13/cm^2. The effect of the HF surface clean before a-Ge DCD is shown in Fig.10 for a-Ge/SOI wafers, top row X-TEM images are with HF surface cleaning and bottom row is without HF clean. The higher SPEC annealing condition with surface cleaning resulted in lower density of defects and further optimization of annealing such as using advanced msec or nsec annealing techniques is preferred but was not available in 2004. Good pMOS devices with a high-k/metal gate first approach were achieved with this technique but poor nMOS devices due to poor n+ S/D activation requiring a high-k/metal gate last approach as shown in Fig.11a (17). Localized high mobility Ge-channels could be formed by Ge DCD directly into the channel region thereby leaving the n+ S/D regions composed of Si material for high n+ dopant activation and shallow junction formation avoiding poor activation and enhanced diffusion of n-type dopant in Ge. Today, the industry has moved from planar 2-D devices (except for FD-SOI) to 3-D FinFET devices for smartphone application processor requiring a change to the original proposal to where the Ge or SiGe Fin region is first formed then the n+S/D region is recess etched away and Si-SEG is selectively grown and then doped n+ by implantation leaving just Ge in the channel/Fin region shown in Fig.11b (12). The original 2-D approach can still be used for FD-SOI planar devices with gate-first or gate-last options.



a) b)

Fig.6: Patterned photoresist SEM image of a) before and b) after 200nm a-Ge DCD.

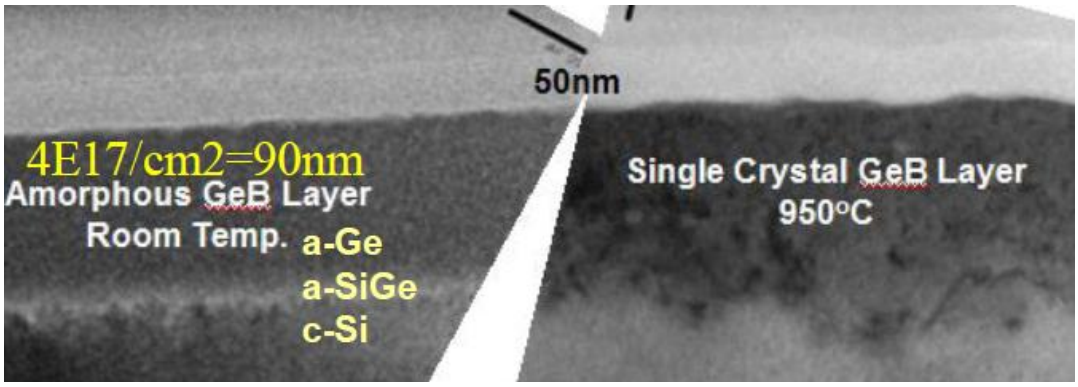


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Fig.7: X-TEM of 4E17/cm^2 DCD of 90nm a-Ge a) before and b) after SPEC annealing.

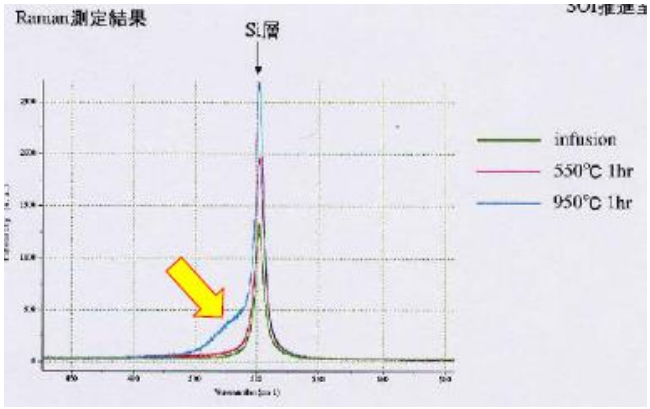


Fig.8: Raman analysis showing tensile strain-Si after a-Ge DCD SPEC annealing.

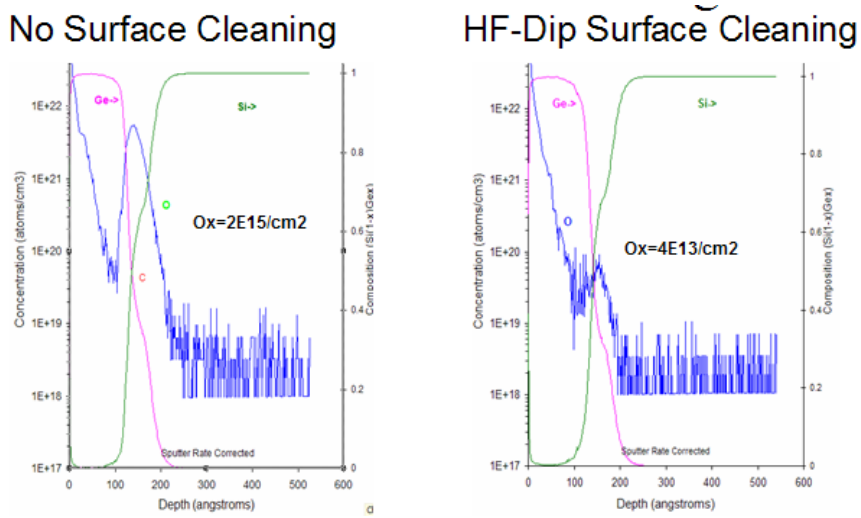


Fig.9: SIMS interfacial oxide analysis for 12nm a-Ge DCD with and without HF surface clean.

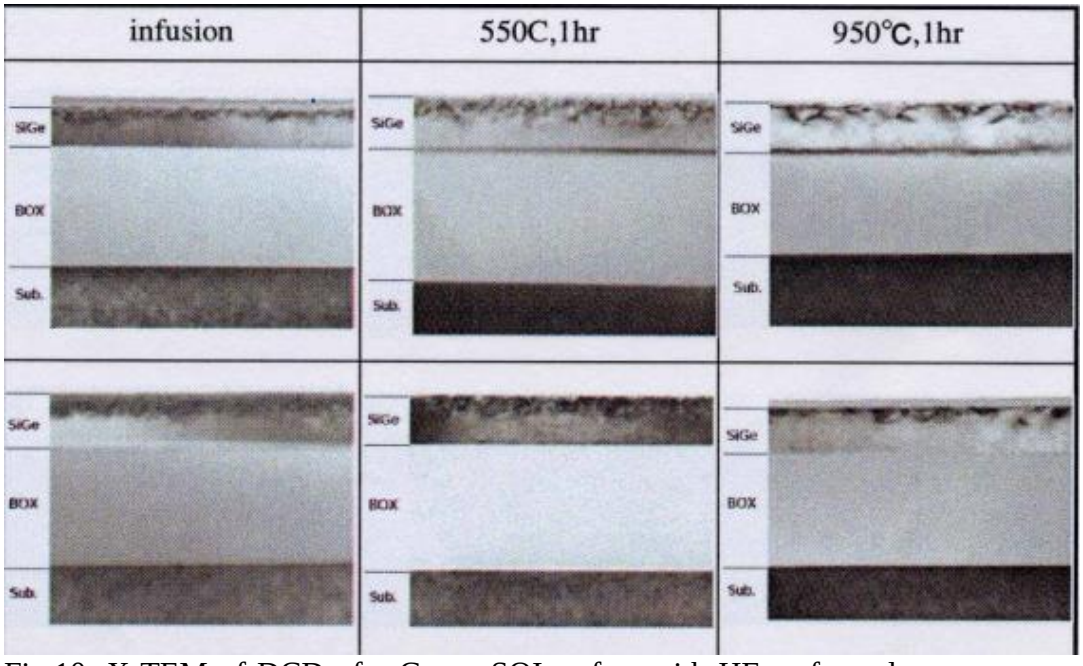
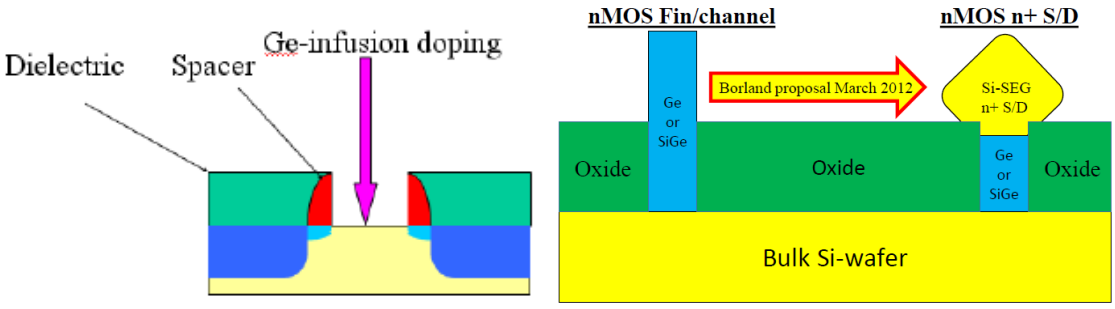


Fig.10: X-TEM of DCD of a-Ge on SOI wafers with HF surface clean top row and no surface cleaning bottom row before and after SPEC annealing.



a) b)

Fig.11: a) Planar Ge nMOS using Ge channel formation by gate last approach and b) nMOS Ge-FinFET were Ge Fin/channel and Si-epi for n+S/D region.

At IWJT-2013 Borland et al. reported using Ge-plasma ion implantation at 1E16/cm^2 and 1E17/cm^2 doses with selective/localized 308nm and 515nm laser melt annealing to realize high quality up to 55% Ge epilayer by LPEC with >4x higher μ_h (160cm^2/Vs) measured by Differential Hall layer mobility in Fig.12 due to the surface tensile strain-Si+Ge XRD plot in Fig.13 with high >25% Ge surface level shown in the Ge-SIMS of Fig.14 (18). Using LPEC rather than SPEC annealing no residual implant damage or EOR defects remained when the laser melt depth exceeded the a-Ge depth of 60nm as shown by the X-TEM in Fig.14. They used therma-wave (TW) analysis to monitor the LPEC process for complete implant damage recovery with epitaxial recrystallization as shown in Fig.15 were the TW value goes from 500K to <5K TW units. One limitation noted with plasma Ge implantation was poor retained Ge dose due to surface sputtering at low energies which limited the Ge content to 55% for the 1E17/cm^2 dose so 100% surface Ge by DCD could not be realized with plasma Ge implantation, 1E16/cm^2 Ge dose achieved 20% Ge. To overcome this retained dose problem at the Oct 2014 ECS meeting Borland et al. reported on Ge beam-line ion implantation to achieve higher retained dose for precise controlled a-Ge deposition by DCD (19). A 5E16/cm^2 Ge implant dose resulted in a 7.5nm thick a-Ge deposited surface layer followed by LPEC using laser melt annealing to form tensile strain-Si+Ge layers improving μ_e by 1.5x. Fig.16 shows LPEC control of the laser annealing melt depth to <15nm as revealed by the O-SIMS profiles for the 7.5nm a-Ge DCD by beam-line implanter.

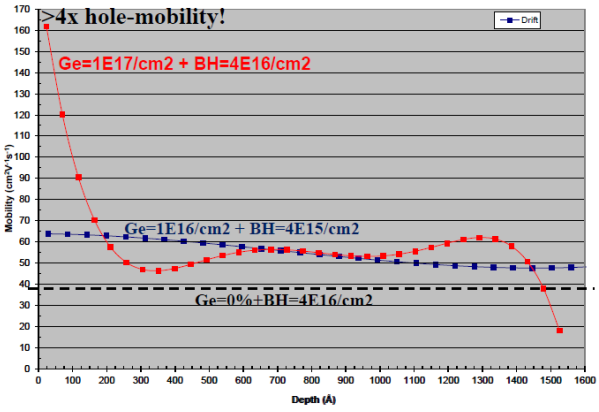


Fig.12: Differential Hall showing 4x μ_h.

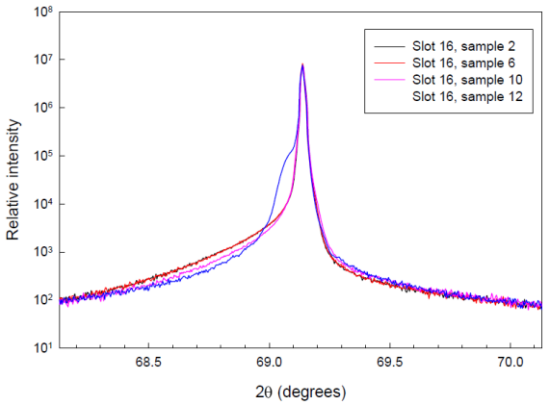


Fig.13: XRD of tensile strain-Si+Ge.

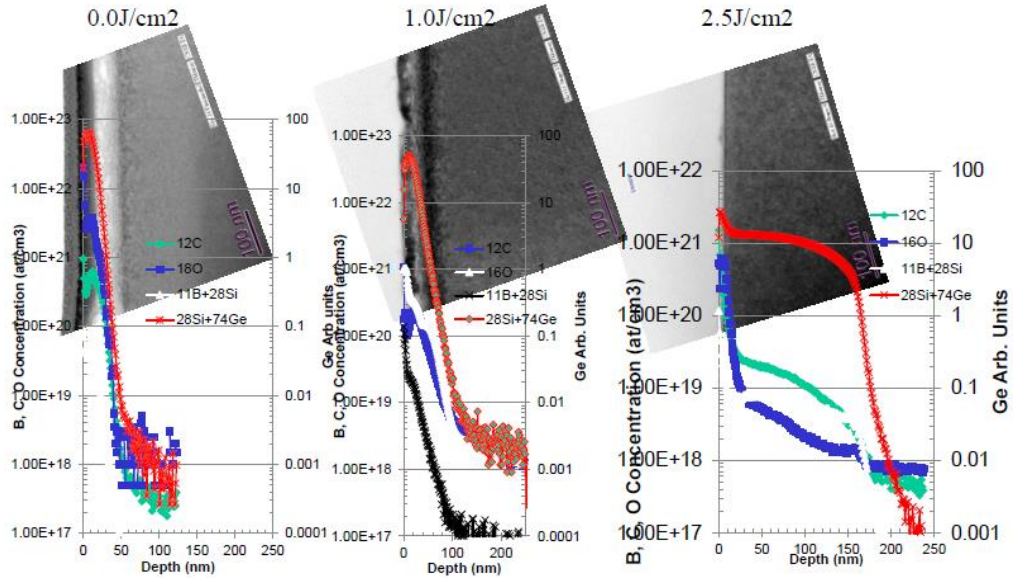


Fig.14: SIMS and X-TEM analysis for various laser power anneals.

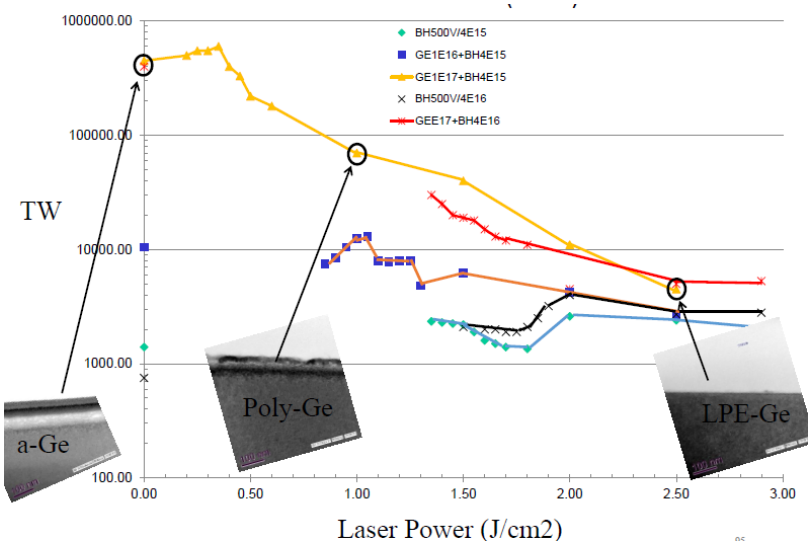


Fig.15: TW analysis and X-TEM showing plasma Ge implant damage recovery after LPEC.

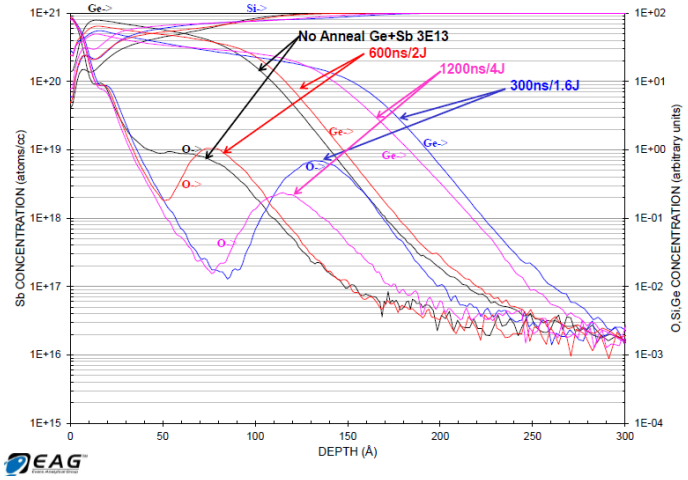


Fig.16: Ge and O SIMS depth profiles for shallow <15nm LPEC.

GeSn Formation

The traditional method to form high mobility GeSn channel material is again by CVD epitaxial deposition with the high TDD and therefore poor junction leakage. At IWJT-2015 Borland et al reported on an alternative method using amorphous Sn (a-Sn) ion implantation followed by LPEC nsec annealing (20). From the lattice constant data in Fig.1 Ge is 5.64Å while Sn is 6.48Å, 13% larger. 14% Sn would be the same 3.8% lattice constant increase as going from Si to Ge so they investigated 10% Sn implantation into Ge-epi on Si wafers. Fig.17 shows the Sn-SIMS profile in Ge-epi after 308nm laser annealing. Differential Hall shows a 2x μ_e improvement for Sb doped n+ Ge junctions while Phos doped n+ Ge junctions showed no improvement but degradation in μ_e. Fig.19 shows the XRD analysis results for Sn implant into Ge-Cz wafer with the Ge peak shoulder/hump to the left of the Ge main peak due to tensile strain-Ge+Sn and in the p-well regions the μ_h was 400cm^2/Vs while in the n-well regions μ_e increased by 2.5x from 500cm^2/Vs to 1250cm^2/Vs as shown in Fig.20.

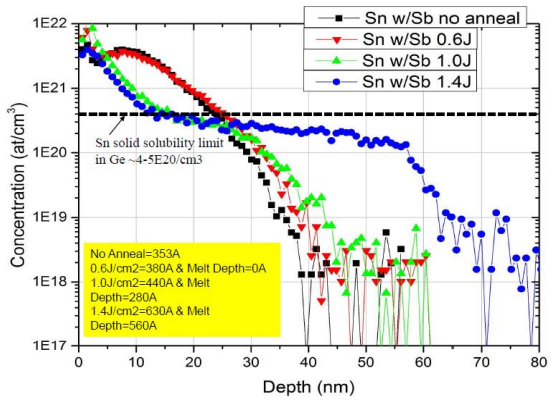


Fig.17: Sn SIMS analysis after LPEC.

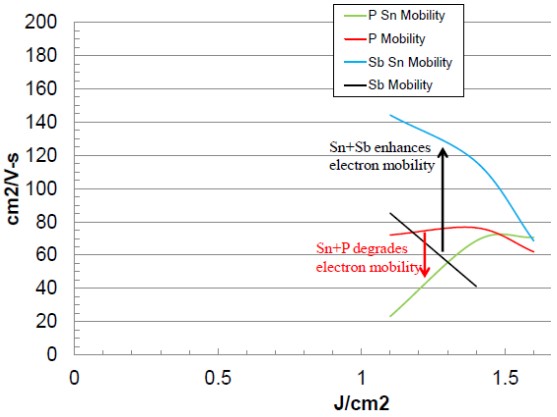


Fig.18: Differential Hall μ_e for n+ Ge.

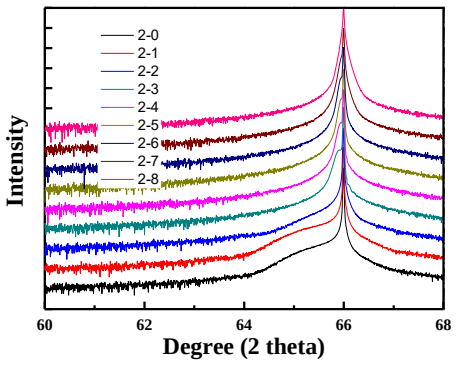


Fig.19: XRD of tensile strain-Ge+Sn implant.

Fig.20: Ge+Sn Cz wafer improves μ_e 2.5x.

SiC Formation

The lattice constant for C as shown in Fig. 1 is 3.56Å so compared to Si 5.43Å a 35% shrinkage in lattice size. The equivalent -3.8% Si lattice shrinkage (5.43Å-0.21Å=5.22Å) for 100% Ge +3.8% lattice increase (5.43Å+0.21Å=5.64Å) would require SiC with 11.2% C_{sub}. Solid solubility of C in Si at melt point is only 3.5E17/cm^3 or about

0.001% so most studies target <2% C_{sub} for a -0.7% Si lattice constant change for compressive strain-Si.

From 2007 to 2010 there have been several interesting publications on using C-implantation to form eSiC NMOS S/D stressor using SPEC of the amorphous SiC S/D region. Liu et al in 2007 reported forming SiC Source/Drain (S/D) stressor by implanting C into an amorphized Si layer and regrowing it with SPEC to form SiC on their 65nm bulk CMOS process at IBM (4). XRD analysis showed C_{sub}=1.65% for S/D compressive strain-Si and convergent beam electron diffraction (CBED) determined the channel tensile strain-Si to be 615MPa. This tensile channel strain improved NMOS Si μ_e by 35%. For comparison they also applied SiC-S/D stressor to PMOS and the tensile channel strain degraded Si μ_h by 60%.

A year later at SSDM-2008 Koh et al reported their results on SiC-S/D stressor using Cluster-Carbon with Excimer laser (248nm) induced SPEC and LPEC (21). Using a C effective dose of 8E15/cm^2 they achieved C_{sub} of ~1.1% for compressive SiC-S/D stressor at the narrow optimized laser anneal power of 3.75J/cm^2, at higher laser power the Ge melt degraded C_{sub}. The channel tensile strain-Si improved μ_e by 28%.

In 2009 Itokawa et al. of Toshiba reported on the effects of SPEC annealing on C_{sub} level for 3.6% and 2% peak amorphous Cluster-Carbon implant (22). For the 3.6% peak C case, 5 sec RTA annealing at temperatures from 750^{o}C to 1000^{o}C resulted in C_{sub} level varying from 0% to maximum of 1.4% in Fig.21a. The 1.4% C_{sub} was achieved for the lowest temperature 750^{o}C RTA based on the XRD SiC peak position though the peak intensity was very low while a much sharper SiC XRD peak was achieved for the 850^{o}C RTA at 1.0% C_{sub} level. At higher RTA temperatures the SiC peak moves to the left and is superimposed with the Si peak as a shoulder-hump to the right of the Si peak suggesting compressive strain-Si. Switching to msec non-melt laser annealing at 1300^{o}C the C_{sub} level increased to 2.0% for both low and high C peak as shown in Fig.21b.

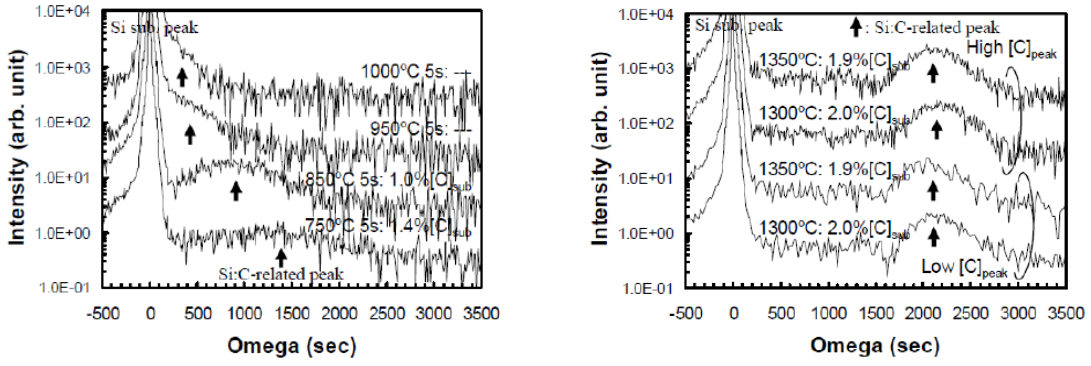
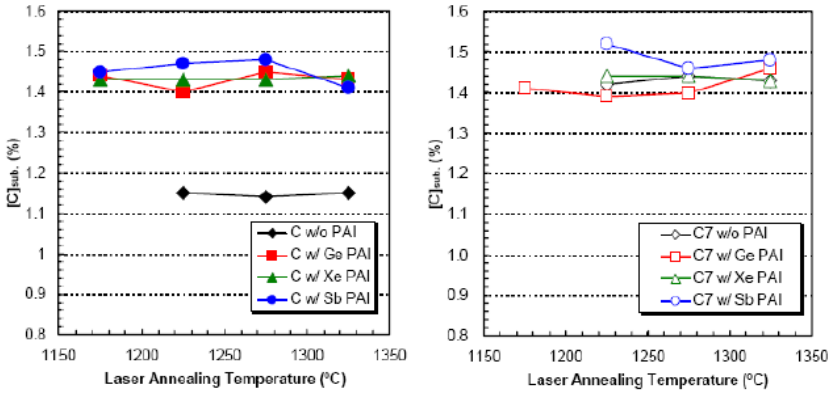


Fig.21: XRD analysis showing Si+C formation by cluster-C implantation after SPEC anneal by a) low temperature RTA and b) high temperature non-melt laser annealing.

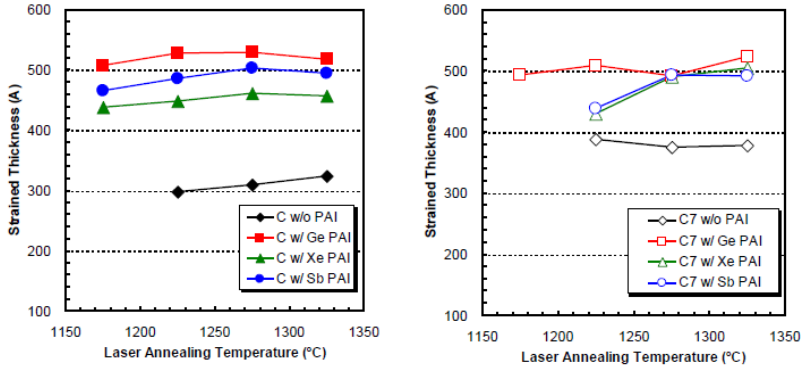
Also in 2009 at the IEEE-RTP conference Borland et al. reported on monomer-C and cluster-C implantation with non-melt laser annealing (9). With a C implant dose of 5.5E15/cm^2 the maximum C_{sub} achieved was 1.15% with monomer-C while with self-amorphizing cluster-C, 1.43% C_{sub} was realized. Fig.22 shows the C_{sub} values versus laser annealing temperature. The compressive strain-Si+C depth is deeper with deeper amorphous depth as shown in Fig.23. Ge-PAI resulted in the deepest strain-SiC depth

but Sb-HALO amorphization gave the highest C_{sub} value of 1.52%. Therma-wave measurement was used to monitor the C implant damage recovery after SPEC msec annealing as shown in Fig.24. Cluster-C had lower residual implant damage than monomer-C and Ge-PAI had the lowest residual implant damage.



a) b)

Fig.22: Csub level in Si+C implanmtation using a) monomer-C or b) cluster-C.



a) b)

Fig.23: Strain-Si+C depth using a) monomer-C or b) cluster-C implantation.

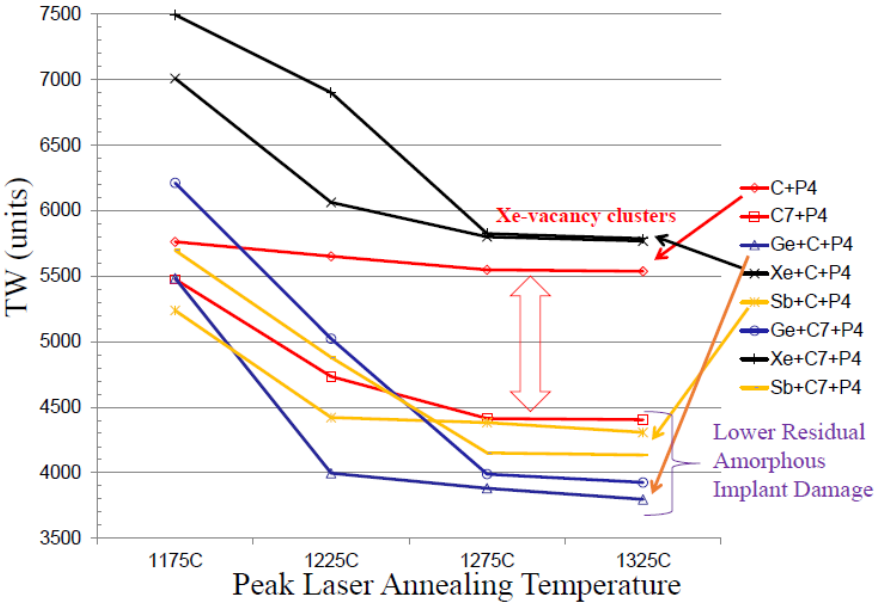


Fig.24: TW analysis of Si+C implant damage recovery after SPEC annealing.

Summary

Localized tensile and compressive strain-Si and strain-Ge channel material for high electron and hole mobility can be fabricated without the high threading dislocation density degrading junction leakage observed with SiGe or Ge epi techniques by using dose controlled Ge, Sn or C ion implantation with optimized SPEC or LPEC advanced annealing techniques. Tensile strain-Si+Ge improved Differential Hall μ_h by 4x and μ_e by 1.5x while tensile strain-Ge+Sn improved μ_e by 2-2.5x. Also Ge-Cz wafers appear to have higher mobility than Ge-epi on silicon wafers suggesting the high density of TD in Ge-epi is degrading mobility. New studies using n-well and p-well doped regions are currently being investigated for Si+C, Si+Ge, Si+Ge+Sn, Si+Sn, Ge+C and Ge+Sn making this approach very attractive for both 3-D FinFET or nanowire devices as well as traditional 2-D planar FD-SOI and 3-D stacked devices at 7nm node and beyond.

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