

Flash Annealing Technology for USJ: Modeling and Metrology

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Millisecond annealing either by flash lamp or laser appears to be the leading approach to meet the needs of ultra-shallow junction annealing and polysilicon activation for advanced technology nodes. There are many advantages to this technology including high electrical activation, excellent lateral abruptness, controlled and limited dopant diffusion and the ability to engineer the extended defects remaining from the ion implantation. There are also many challenges such as potential pattern effects, local and global wafer stress and difficulty in process integration. Additional challenges include the need to extend the capabilities of process TCAD to allow accurate simulation and prediction of the ms processes. Modeling of diffusion, activation and defect evolution for a variety of technologically interesting doping conditions must be dependable to allow the device designer and process engineer to predict the device behavior after ms annealing. Existing models fall short or still need to be validated. Metrology for ultra-shallow junctions is also a challenge. The ability to accurately and repeatably measure sheet resistance and junction leakage on junctions of the order of 10nm deep is very difficult.

This paper will provide an overview of flash lamp annealing and deal with some promising extensions of process simulation to enable the predictive modeling of junction behavior under flash lamp annealing conditions. We will also examine some of the new metrology techniques for characterization of these very shallow junctions and look at some of the trends exhibited for different junction formation details.

INTRODUCTION

Future integrated circuits, especially advanced-logic device technology for the 45nm node and beyond will require highly-activated, shallow, and abrupt dopant profiles [1]. The combination of advanced ion implantation and an advanced annealing technology is expected to provide solutions for these requirements. Conventional annealing technology, such as spike annealing is reaching its limit. An essentially diffusion-less,

but highly activating, high-temperature method such as the various milli-second annealing approaches for the formation of ultra-shallow junctions will be needed. There are several methods to achieve ms duration anneals including at least three approaches to laser annealing and flash lamp annealing. The flash-assisted RTP™ (fRTP™) technique is a promising method for achieving junction depth and sheet resistance values low enough to meet the performance specifications for the 65 and 45

nm nodes [1]. The optimal process for high activation during flash-assisted RTP involves a temperature ramp-up to an intermediate temperature of 700°C to 900°C and, once the intermediate temperature is reached, a very short, intense flash on the front side of the wafer induces temperature jumps up to approximately 1325°C with a peak width of approximately 1 ms.

In this paper, we will review some of the electrical results on pMOS junctions. (pMOS is investigated since boron is a fast diffuser and meeting the R_s and X_j targets more difficult.) To be useful for device fabrication, it is necessary to understand and be able to predict the behavior of advanced shallow junction activation and annealing, so a practical process TCAD methodology is essential to take full advantage of these approaches. Conventional process TCAD was not designed to predict anneals in the ms regime, so new models and simulation techniques have been developed based on some of the ms annealing results. Some of these simulations will be examined here.

In order to investigate such shallow junctions, new metrology methods are also needed. Conventional four point probe sheet resistance measurements have done a good job of measuring shallow junctions, but the reliability of these measurements as junction depths reach levels below about 20nm begins to suffer due to punch through of the probes. In addition, it is important to look at other parameters besides sheet resistance. Leakage will be very important, especially in devices for low power (e.g. mobile) applications. This paper will also summarize some recent results in looking at new metrology techniques for characterizing ultra-shallow junctions.

EXPERIMENTAL DETAILS

For most of the experiments, 200 mm, n-type 10 – 20 Ω cm, prime (100) Si wafers were used. The samples used were implanted to a nominal dose of $1.0E10^{15}$ cm^{-2} with either $^{11}\text{B}^+$ (0.5 keV) into crystalline silicon or with a $^{74}\text{Ge}^+$ preamorphized layer (10 keV or 30 keV $1.0E10^{15}$ cm^{-2}). For the former, a drift implantation mode was used in

some cases to minimize the tail normally observed in implants performed with deceleration. Some advanced doping techniques were also used. BF_2 , $\text{B}_{10}\text{H}_{14}$ and $\text{B}_{18}\text{H}_{22}$ molecular implants were used to provide very shallow junctions to test the metrology. The flash anneal process was performed at various peak temperatures, T_p , typically 1275 to 1325°C with intermediate temperatures, T_i , of 700°C to 825°C. For all anneals the gaseous ambient was N_2 with 100 ppm partial pressure of O_2 . For comparison some wafers were annealed with an optimized 1050°C spike anneal recipe 0. The full wafer sheet resistance mapping was performed on a KLA Tencor RS100 using a D-type probe and 7 mm edge exclusion as well as newer techniques to be described later. The dopant atom distributions in the flash-annealed samples were analyzed by high resolution secondary ion mass spectrometry (SIMS) at FEI Germany (FEI SIMS 4600 quadrupole depth profiler, 0.5 keV O_2 beam at normal incidence for boron and a 0.5 keV Cs beam at a 45° oblique mode for arsenic). Precise depth calibration was carried out by using delta-doped samples, and concentration calibration by using uniformly doped standards 0. Under these conditions the dose measurement repeatability is typically within 1% (1σ , RSD) and the repeatability of junction depth measurement within $\pm 1\%$. The chemical junction depth throughout this publication is defined as the depth where the total boron or arsenic concentration falls below a level of $5E10^{18}$ cm^{-3} in the SIMS profile for the 65 nm technology node or $7E10^{18}$ cm^{-3} for the 45 nm node, respectively.

RESULTS

The reason that ms annealing techniques are needed is that the activation energies for the undesired boron dopant diffusion are different from the desired activation energies for defect removal and electrical activation. This difference in activation energies implies that short, very high temperature processes will favor the desired processes over the undesired ones. Even with spike anneals of 200 ms peak width, the elimination of ordinary diffusion was not

possible [2,3]. Milli-second annealing reduced the peak width to ~ 1.6 ms thereby having the advantage of heating only the top layer and using the residual bulk as heat sink. This leads to the expected advantages. Figure 1 shows the major reduction in junction depth that is possible by activation with anneal times that range from seconds to milliseconds. As an alternative, the low temperature approach for forming activated, “non-diffused” junctions by the solid phase epitaxial growth (SPEG) process is also shown in Figure 1. The spike anneal process with a peak temperature of 1050°C (time duration above $1000^\circ\text{C}=1.27$ s) still shows in both amorphous and crystalline silicon case broadening due to ordinary diffusion. Although the use of co-implanted species such as fluorine or carbon can lead to shallower, highly activated profiles with spike anneals, this only helps slightly and can have some undesired side effects such as increase in junction leakage. The boron profiles in the pre-amorphized layer show, for both spike and flash annealed samples, a stronger transient-enhanced diffusion effect which leads to a deeper junction even though the as-implanted profile is shallower. All annealed profiles show a kink in the concentration profile at around 6 nm, separating the apparently immobile peak from the diffusing tail. For convenience the concentration level at the kink position will be referred as effective “chemical” solubility limit, C_{chem} , which continuously decreases from flash anneals ($3.6E10^{20}$ cm^{-3}) through SPEG ($2.1E10^{20}$ cm^{-3}) to spike anneals ($1.4E10^{20}$ cm^{-3}).

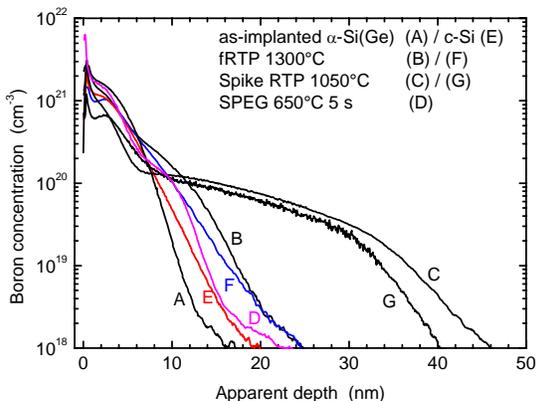


Fig. 1: SIMS profiles of as-implanted 500 eV boron in Ge pre-amorphized (A) and crystalline silicon (E) as well as flash-annealed (1300°C , B, F), spike-annealed (1050°C , 0 s

250 K/s, C, G) and SPEG-processed (650°C , 5 s, D) are shown. In case of (E) the implanter’s drift mode was used. The gaseous ambient for all thermal processes was 100 ppm of oxygen in nitrogen 0. B: 423 Ω/sq .; C: 408 Ω/sq .; D: 756 Ω/sq .; F: 578 Ω/sq .; G: 460 Ω/sq .

Flash-annealing of boron doped pre-amorphized silicon

Figure 2a shows the TED effect for flash anneals in the case of pre-amorphized (α -Si) substrates. An increase of the peak temperature by 100K at the same intermediate temperature leads only to a marginal increase in the diffusion length. But elevating the intermediate temperature from 700°C to 825°C increased the junction depth by 2 nm and decreased C_{chem} to $3.3E10^{20}$ cm^{-3} . This effect can be explained by an augmented diffusion of silicon self-interstitials from the EOR damage towards the boron-implanted layer while reaching the elevated intermediate temperature. A reduced activation is also apparent from the sheet resistance values. For the same peak temperature of 1300°C the sheet resistances are 423 Ω/sq . for the intermediate temperature of 700°C , and 443 Ω/sq . for the intermediate temperature of 825°C . Enhanced deactivation with increasing temperature has been reported already for SPEG [8]. It is associated with the dissolution of EOR damage (see Figure 2b) during the very high, but extremely short annealing temperatures. The defect population after the thermal process has already transformed to faulted and perfect dislocation loops (f-DLs and p-DLs, respectively). From a comparison of the annealing schemes (B to D) a significant increase of the defect size can be noted and, at the same time, a significant decrease of the defect density. Both observations are in qualitative agreement with a non-conservative Ostwald ripening process. Moreover, a progressive evolution of p-DLs towards the more energetically stable f-DLs is clearly visible. In the case of an increased intermediate temperature (E) the defect density at similar size is decreased compared to (C) which supports the contention that the deactivation is driven by EOR dissolution for this annealing condition. It is important to note that flash annealing, despite

the very high temperature, does not fully dissolve the defects in the crystal, probably due to the very short time scale of the flash.

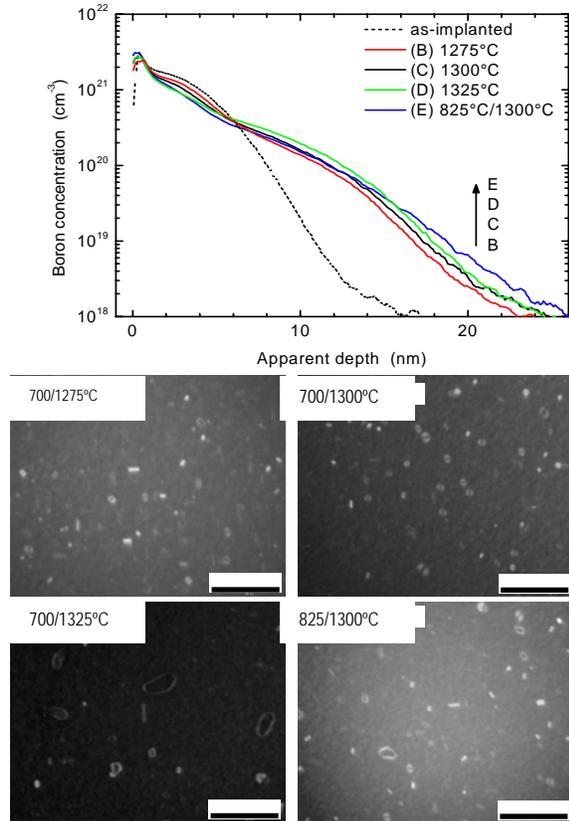


Fig. 2: (a) Dependence of boron redistribution in pre-amorphized silicon on the peak and intermediate temperatures. B, (700°C/1275°C): 462 Ω/sq.; C (700°C/1300°C): 423 Ω/sq.; E (825°C/1300°C): 443 Ω/sq.; D (700°C/1325°C): 368 Ω/sq. (b) Weak beam dark field plan-view micrographs of flash-annealed samples of (a) to study the effects of the temperature profiles on the evolution of defects.

In summary, the electrically active dose, as well as the surface concentration, increase with temperature. At the same time, despite the temperature increase, the junction depth is only weakly increased (“diffusion-less process”). All of this would suggest that mobility decreases, 0 but the mobility was also found to increase (see Figure 3a). Therefore it can be concluded that the quality of the crystal improved. It should be noted that this does not necessarily mean a reduction of EOR defects because these are far away from the junction and have only an indirect influence on its electrical characteristics.

For the sample with an elevated intermediate temperature of 825°C, the sheet resistance and mobility (39 cm²V⁻¹s⁻¹) increase on the one hand and the electrically active dose (-10 %) and surface concentration decrease on the other. In this case the mobility increase is likely due to a reduction of the electrically active dose as is also seen in the sheet resistance

Flash annealing of boron-doped crystalline silicon

These samples evaluated by TEM exhibit no EOR defects due to the 500eV boron implantation itself. But some small defects have been observed in plan view TEM which are probably located in the depth of the immobile boron peak. Similar defects have been reported previously by Cristiano et al.[9]. Despite the high temperature during flash annealing, these defects are not fully dissolved.

As for ultra-shallow junctions in amorphous silicon, a similar picture for the electrical characterisation can be drawn for crystalline substrates (see Figure 3b). The sheet resistance values deduced from Hall-effect measurements correspond extremely well to the 4PP ones. The deviations between the values are below ±1% which shows that the penetration of the 4PP tips is shallower than the pn-junction. The mobility in the crystalline case is about 40 cm²V⁻¹s⁻¹ for the various samples despite the increase of the electrically active dose. This is much higher than the best value in pre-amorphized samples and indicates less scattering due to centers over the entire temperature range.

The electrical activation in α-Si by flash anneals is less dependent on peak temperature than the electrical activation in crystalline silicon. On the other hand, spike anneals exhibit extreme sensitivity to peak temperatures ranging from 950°C to 1100°C. The SPEG process activates 30% less boron compared to a 1300°C flash anneal. So, overall, the flash anneal is the most promising candidate because it combines the SPEG process up to the intermediate temperature with the advantages of high temperature activation. This is the most suitable approach for the highest electrical activity combined with the shallowest boron junction below 25 nm.

The evolution of the electrically active dose obtained from Hall-effect measurements upon annealing at 800°C is reported in Figure 3. The asymptotic reduction in the active dose but the continuous increase in mobility with time as competing processes show that no real activation occurs during this time regime up to 900s. The former effect indicates a continuous formation of clusters so that the decrease in sheet resistance is solely attributed to the improved mobility which is in turn, a consequence of the diffusion-broadening of the profile. This is different from the SPEG experience where a reactivation occurs at times longer than 120s by increasing of the active dose ρ i.e. a dissolution of clusters takes place.

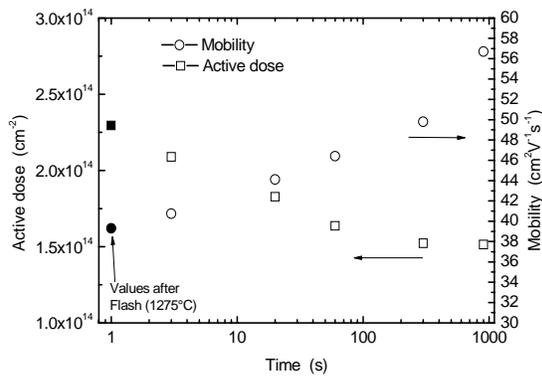


Fig 3: Mobility and active dose versus post-annealing time at 800°C. The solid symbols denote the value after flash annealing with an intermediate temperature of 700°C and a peak temperature of 1275°C.

It is interesting to note also for these data, that the sheet resistance values measured via Hall-effect corresponds to the measured 4PP sheet resistance value within $\pm 3.9\%$.

Finally, Figure 4 shows the evolution of the sheet resistance of 1300°C flash-anneal activated junctions during isothermal anneals in the temperature range 750°C to 900°C. The results indicate that with longer post-annealing times more or less deactivation occurs at all temperatures. Also the decrease in sheet resistance (no real activation) at longer post-annealing times depends on temperature. The deactivation rate weakly depends on temperature whereas the sheet resistance decrease strongly depends on temperature, indicating that the mechanism is thermally activated. The sheet

resistance decrease of the boron upon annealing is characterized by boron clustering (reduction of electrical active dose) with a continuous mobility increase. This is different from the α -Si case where the competition between boron clustering (deactivation) versus cluster dissolution and dopant diffusion (reactivation) takes place and the electrically active boron dose increases.

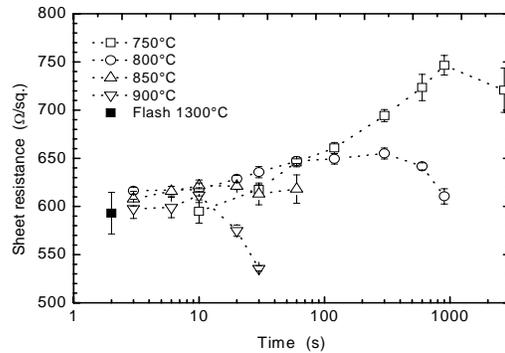


Fig. 4: Sheet resistance vs. annealing time for boron flash-activated junctions (1300°C) in crystalline silicon after isothermal post-annealing for various times. The solid square denotes the sheet resistance value of the 1300°C flash-activated junction.

PROCESS SIMULATION

As part of the EU funded ATOMICS program, work has been done to simulate flash annealing of boron into crystalline and Ge pre-amorphized silicon. Some of the work on simulating the crystalline Si implants is presented here [10]. For the simulations shown in Figure 5, the B312 model described in reference 10 was used. The anneal conditions in this figure are a flash anneal with an intermediate temperature of 700°C and peak temperatures of 1270 and 1340°C respectively. Excellent agreement in both cases for both the chemical dose profiles and the total electrically active dose (determined by Hall Measurements at CEMES-LAAS/CNRS in Toulouse, France by A. Clarverie and F. Christiano)

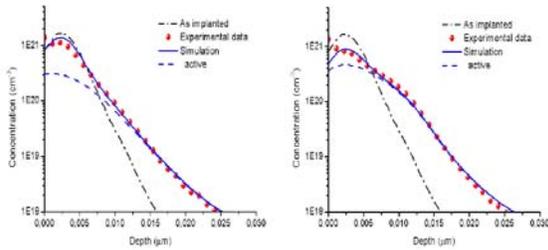


Figure 5: Comparison of the simulation and experimental data for fRTP anneals of 500eV, 1E15cm-2 boron in crystalline silicon with peak temperatures of 1270°C (left) and 1340°C (right).

This early simulation result is very promising and work is now ongoing to simulate boron implantation into pre-amorphized silicon.

ADVANCED METROLOGY

As junction become shallower, traditional metrology methods become increasingly difficult to use. For example, contact four point probe (4PP) measurements have been used to measure sheet resistance for many years. Due to the very thin active layer in ultra-shallow junctions, it is often difficult to use conventional 4PP without obtaining errors due to the penetration of the probe through the junction. The high leakage present in some ultra-shallow junctions also leads to significant measurement errors and, in extreme cases, to the measurement of the substrate resistivity rather than the active region's.

Several new technologies to measure sheet resistance have been developed in recent years that use either non-penetrating contact or no contact at all. Among these are the use of mercury four point probes [11], elastic material four point probes [12] and the contactless RsL technique [13] which also gives an indication of junction leakage as well as sheet resistance. These methods were utilized in a related study [14] and it was found that there is generally good agreement among the techniques. Figure 6 shows the Rs results of the 4 advanced metrology techniques on many different samples with different doping and annealing methods applied. There is excellent correlation except in a few cases (circled).

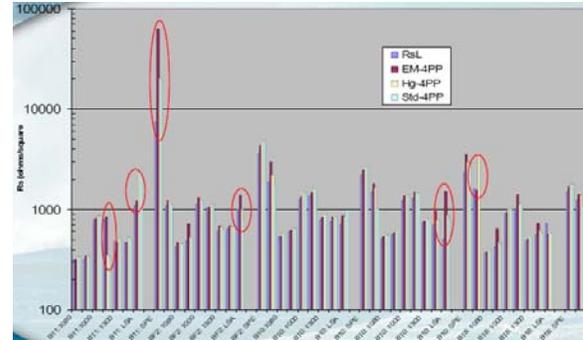


Figure 6: Comparison of Rs measurement techniques using standard contact 4PP, mercury 4PP, elastic material 4PP and RsL. Circled data indicates only data points not well correlated. [14]

In addition to the difficulty in accurately measuring sheet resistance, the use of SIMS to accurately measure the chemical dopant profile has also become more challenging. It is important to use the correct SIMS protocols when measuring ultra-shallow junctions.

As mentioned previously, ms annealing alone will generally not remove all of the extended defects resulting from a pre-amorphized implantation. Since the remaining extended defects can be a source of junction leakage, it is important to investigate this aspect of the junctions. Traditionally, diodes are formed and either contacts are evaporated or a mercury probe is used to measure junction leakage. These methods are time consuming, destructive and not particularly reliable. The FSM RsL method of sheet resistance measurement will also give an indication of junction leakage. Although the parameter measured is not strictly the reverse biased leakage usually considered, the near zero biased leakage does correlate very well to the reverse bias case. Table 1 below shows the RsL leakage for the cases shown in Figure 6.

Dopant	Spike/1080	Spike/1000	Flash/1300	Laser/1300	SPE/650
B11	1E-7	1E-7	1E-7	3E-7	1E-5
wPAI	1E-7	1E-7	1E-7	2E-2	6E-6
Bf2	1E-7	1E-7	1E-7	3E-6	1E-6
wPAI	1E-7	1E-7	1E-7	1.5E-3	1E-5
B10-serial	1E-7	1E-7	1E-7	2E-7	2E-7
wPAI	1E-7	1E-7	1E-7	1.8E-3	3E-5
B10	1E-7	1E-7	1E-7	1E-7	2E-7
wPAI	1E-7	1E-7	1E-7	2.3E-2	3E-5
B18	1E-7	1E-7	1E-7	1E-7	2E-7
wPAI	1E-7	1E-7	1E-7	2.3E-2	2E-6

Table 1: RsL leakage measurements from ref [14]

It is interesting to note that with all implant conditions, the spike and flash anneals show very low leakage, but the laser and SPEG anneals have some cases that show much higher leakage.

SUMMARY AND CONCLUSIONS

In this paper the flash anneal process for PMOS is discussed. $500\text{eV } 1\text{E}10^{15}\text{ cm}^{-2}$ boron in pre-amorphized as well as crystalline samples were implanted and flash-annealed. From a sheet resistance point of view the junctions satisfy the 65 nm node but unfortunately the junction depth does not due to too deep as-implanted profiles. All these junctions withstand, without sheet resistance degradation, a thermal cycle for NiSi self-aligned silicide formation. However the evolution of the sheet resistance together with the evaluation of Hall and TEM measurements suggest that the deactivation/reactivation process during post-annealing sensitively depend on the morphology of the starting substrate (c or α -Si). In the case of crystalline material the reactivation is due to strong competition between mobility increase and electrical dose decrease whereas in pre-amorphized substrates the reactivation is a true increase in active dose. The combination of several measurements techniques allows separation of the various effects to clarify the various mechanisms. It is interesting to note that both Hall and four-point probe measurement agree very well within $\pm 3.9\%$.

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