45nm Node p+ USJ Formation With High Dopant Activation And Low Damage

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Abstract

We investigated various p+ extension implantation dopant species (B, BF_2, $B_{10}H_{14}$ & $B_{18}H_{22}$) and annealing techniques (spike, flash, laser and SPE) to achieve high dopant activation low damage ultra-shallow junctions (USJ) 15-20nm deep for 45nm node applications. New USJ metrology techniques were investigated to determine: 1) surface dopant activation level and 2) junction quality (residual implant damage) using contact and non-contact full wafer metrology methods. We discovered that using molecular dopant species ($B_{10}H_{14}$ & $B_{18}H_{22}$) either high temperature (flash or laser) annealing or low temperature SPE annealing are very promising for the 45nm node process integration with SiON or high-k Hf-based dielectric gate stack structures because of their wide temperature range for dopant activation without diffusion.

1. Introduction

For the 45nm node, the p+ USJ for extension varies between 15nm to 20nm deep depending on the device application and trade-offs between dopant activation, junction depth (Xj) and junction quality for high performance (HP), low operating power (LOP) and low-standby power (LSTP) logic devices. To minimize boron dopant diffusion, high temperature >1300^{o}C (flash or laser) or low temperature 650^{o}C SPE annealing are available resulting in 0 to 5nm of dopant movement. To eliminate dopant channeling pre-amorphization implantation (PAI) is usually used. PAI and/or co-implantation can lead to higher dopant activation, however, the residual end-of-range (EOR) damage can also result in high damage junctions when using these advanced dopant activation techniques with minimal dopant diffusion [1,2]. For this reason we investigated alternative p+ dopant species such as $B_{10}H_{14}$ and $B_{18}H_{22}$ because of their self-amorphization effects avoiding PAI and EOR damage resulting in low damage high quality junctions [3].

Another benefit of using molecular dopant species is the ability to extend beam-line implantation for several more device generations by avoiding decel-mode implantation (energy contamination) and spot beam blow-up effects which has been reported to result in L_G & V_T variation and asymmetrical transistors [4]. Since the low boron solid solubility limit in silicon is usually 10 to 100 times lower than the chemical dopant level at the surface the annealing system determines dopant electrical activation level and across wafer uniformity mirrors the anneal signature. For these reasons new metrology techniques to show the implanter and annealing unique signatures are needed to optimize 45nm node USJ processes.

2. Experimentation

Boron 500eV/1E15/cm^2 dose equivalent implants were performed on one hundred, 200mm n-type wafers using B, BF_2, $B_{10}H_{14}$ and $B_{18}H_{22}$ implant species. The implants were performed into crystalline silicon or 11.5nm deep amorphous silicon layer using Ge 5keV/5E14/cm^2 for PAI. Both batch and serial implanters were used for implant signature comparison. Dopant activation was achieved using: 1) spike annealing at 1080^{o}C or 1000^{o}C at Mattson/Germany, 2) msec flash annealing at 1300^{o}C at Mattson/Canada, 3) 200nsec sub-melt laser annealing at Sopra/France and 4) 5sec 650^{o}C SPE annealing at Mattson/Germany. Electrical measurements were made by both contact and non-contact methods for dopant activation, junction depth and junction quality measurements. Sheet resistance (Rs) was measured with non-contact junction photo-voltage (JPV) at Frontier and contact non-penetrating 4 point probe (4PP) using elastic material (EM) probes at Solid State Measurements (SSM) and mercury (Hg) probes at Four Dimensions (4D). The electrically active surface dopant level/density was measured by a C-V technique (Nsurf) at SSM. SIMS analysis at NEC was used to determine the boron chemical density depth profile and X-TEM to evaluate the amorphous layer depth and after anneal residual implant EOR damage.

After anneal junction quality was determined by junction leakage measurement using JPV at Frontier. Silicon crystal lattice damage levels were measured by photo-luminescence (PL) imaging at Accent on as-implanted and after annealed wafers.

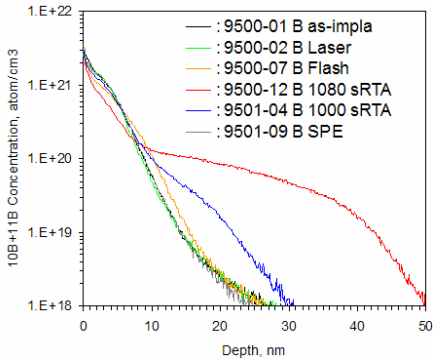
3. Results & Discussion

SIMS boron dopant depth profiles were measured on all the samples. Due to channeling into crystalline silicon, the B case has an X_j of 26.9nm at 1E18/cm^3, while the X_j for the BF_2 case is at 25.1nm, $B_{10}H_{14}$ at 18.7nm and the $B_{18}H_{22}$ case is at 19.7nm. With Ge-PAI, the B case has an X_j at 17.9nm, while the BF_2 case is at 16.6nm, the $B_{10}H_{14}$ case at 14.8nm and the $B_{18}H_{22}$ case at 16.6nm. Table 1 shows all the X_j SIMS chemical junction depth for all the conditions studied, and the amount of dopant movement either positive or negative after each annealing technique. A shallower X_j occurred for some of the diffusion-less activation cases. Figures 1-4 shows SIMS results of the various amounts of boron dopant movement (diffusion) for all the boron species activation/annealing techniques into both crystalline and amorphous silicon.

For the 1080°C spike anneal the deepest junctions were for both the B and PAI+B case with an Xj at 50nm while the shallowest junctions were for $B_{10}H_{14}$ and PAI+$B_{10}H_{14}$ at 36.5nm followed by BF_2 and PAI+BF_2 at 40nm. For $B_{18}H_{22}$ the Xj is at 44.7nm while PAI+$B_{18}H_{22}$ is at 41.1nm. When the temperature was reduced to 1000°C the B and PAI+B cases were again the deepest with an Xj at 30.4nm. However, this time the molecular dopant species with PAI had junctions 3 to 6nm deeper than without PAI (29nm versus 24nm). With flash annealing the B and BF_2 samples with PAI (21nm) were shallower than without PAI (25nm) while the opposite was observed with molecular dopant species, the shallowest junctions were without PAI (18nm) and the deepest with PAI (20nm). With laser and SPE annealing all the samples without PAI had deeper junctions than with PAI

Table 1. SIMS determined Xj depth in nm at 1E18/cm^3 and dopant movement.

Dopant	Control	Spike/1080	Spike/1000	Flash	Laser	SPE/650
B11	26.9	50.1+23.2	30.4+3.5	25.9-1.0	26.8-.1	24.1-2.8
+PAI	17.9	49.3+31.4	30.4+12.5	21.5+3.6	18.0+.1	19.4+1.5
BF2	25.1	40.6+15.5	27.6+2.5	25.2+.1	24.0-1.1	22.0-3.1
+PAI	16.6	39.6+23.0	26.9+10.3	21.0+4.4	17.0+.4	17.7+1.1
B10-serial	18.7	36.5+17.8	23.2+4.5	17.5-1.2	19.8+1.1	17.4-1.3
+PAI	14.8	36.5+21.7	29.3+14.5	19.8+5.0	15.2+.4	16.8+2.0
B10	20.0	36.6+16.6	22.5+2.5	18.6-1.4	19.2-.8	18.0-2.0
+PAI	15.5	36.6+21.1	28.5+13.0	20.9+5.4	15.9+.4	16.9+1.4
B18	19.7	44.7+25.0	25.4+5.7	20.0+.3	21.0+1.3	19.4-.3
+PAI	16.6	41.1+24.5	28.8+12.2	21.6+5.0	16.8+.2	18.2+1.6



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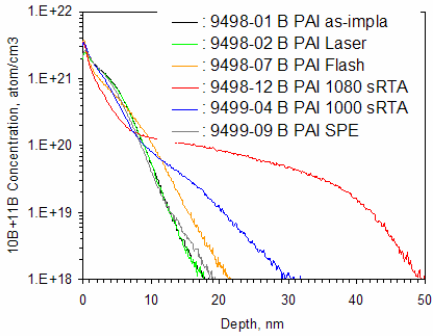

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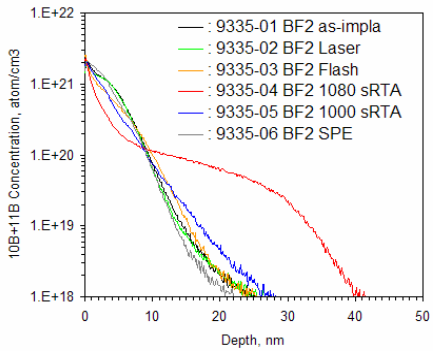
Fig. 1: a) B and b) PAI+B SIMS results.



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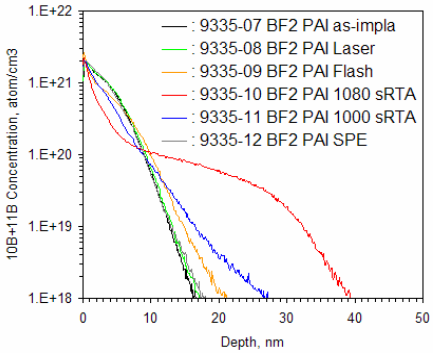

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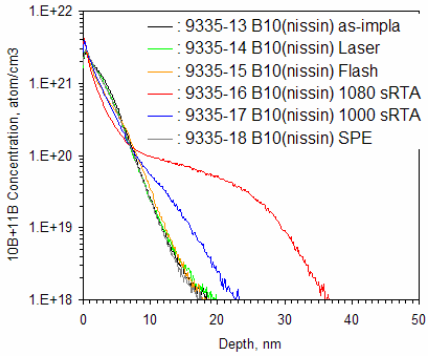
Fig. 2: a) BF_2 and b) PAI+BF_2 SIMS results.



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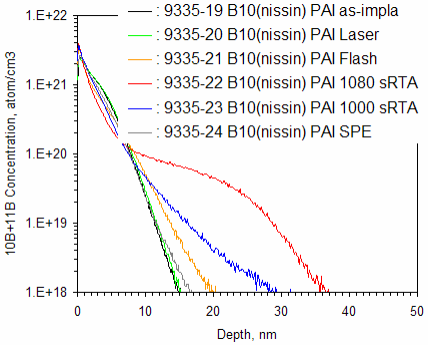

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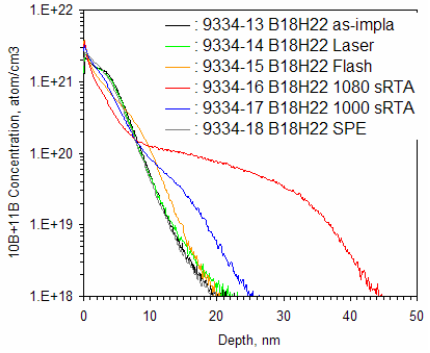
Fig. 3: Serial a) $B_{10}H_{14}$ and b) PAI+$B_{10}H_{14}$ SIMS results.



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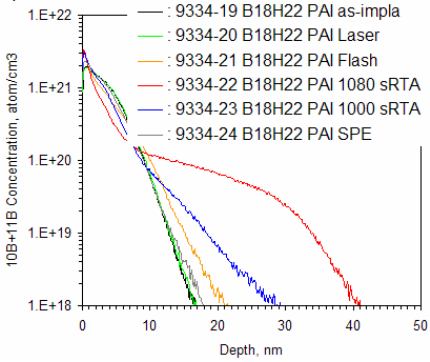

b)

Fig. 4: $B_{18}H_{22}$ & PAI+$B_{18}H_{22}$ SIMS results.

PL analysis was used to get a full wafer image mapping of the as-implanted damage and damage recovery (residual implant damage) after annealing, as shown in Table 2 using arbitrary PL units (APLU). The APLU data clearly shows complete implant damage recovery (low APLU values <16) for the wafers receiving the 1080°C and 1000°C spike anneals, as well as the flash anneals. However, all of the PAI laser annealed wafers still showed high APLU values (55–64), suggesting that a high level of residual implant damage remained.

Table 2. PL results showing damage recovery in APLU.

Dopant	Control	Spike/1080	Spike/1000	Flash	Laser	SPE
B11	46	12	13	8	19	30
+PAI	75	9	10	9	62	31
BF2	41	14	15	11	27	25
+PAI	72	15	16	11	63	27
B10-serial	42	8	9	10	13	14
+PAI	75	10	10	9	64	30
B10	45	9	9	9	12	18
+PAI	74	9	10	10	55	27
B18	46	10	10	9	13	14
+PAI	75	11	11	9	55	29

Also, the BF_2 wafer without PAI had a higher than expected post-laser anneal APLU value of 27, suggesting residual EOR damage (this was verified by X-TEM). This value was similar to the APLU values observed for all the PAI cases with the 650°C SPE anneal as well as the non-PAI B and BF_2 cases. Only the non-PAI SPE annealed $B_{10}H_{14}$ and $B_{18}H_{22}$ wafers showed complete damage recovery with low APLU values. Cross-sectional TEM (X-TEM) analysis on selected B, $B_{18}H_{22}$ and Ge-PAI+$B_{18}H_{22}$ wafers are shown in Figs. 5-7, which provide better interpretation of the PL results. An unexpected result was the B case having a 6.2nm deep amorphous layer as shown in Fig. 5a. This would explain the higher APLU value for B after SPE and laser annealing in Table 2. The $B_{18}H_{22}$ implant also created a 6.2nm deep self-amorphous layer (Fig. 6a), while the Ge-PAI created an 11.5nm-deep amorphous layer (Fig. 7a).

After flash annealing, the APLU values were 9, and the X-TEM showed no residual implant damage (Figs. 6d and 7d). With laser annealing, the $B_{18}H_{22}$ wafer APLU was 13, and the X-TEM was clean (Fig. 6c). Also with laser annealing, the Ge-PAI+$B_{18}H_{22}$ wafer APLU was 55. The X-TEM in Fig. 7c shows an 11.5nm-deep amorphous layer remaining, which indicates that no recrystallization occurred. With SPE annealing, the $B_{18}H_{22}$ APLU was 14 and the X-TEM of Fig. 6b was clean, while the PAI+$B_{18}H_{22}$ wafer APLU was 29 and the X-TEM of Fig. 7b shows EOR damage 12nm deep.

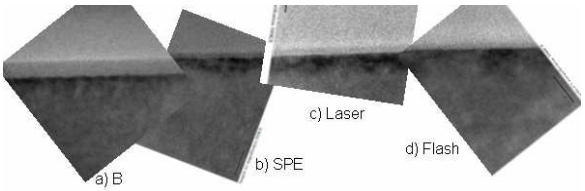

Fig. 5: B X-TEM annealing comparison.

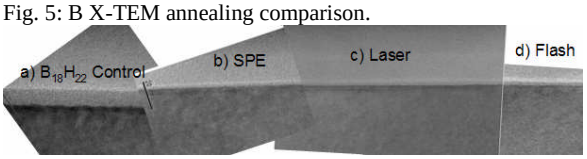

Fig. 6: $B_{18}H_{22}$ X-TEM results.

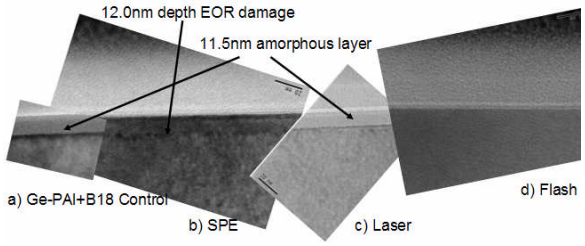

Fig. 7: PAI+$B_{18}H_{22}$ X-TEM results.

The unique signature of each annealing technique can be seen by full wafer PL imaging as shown in Fig. 8. The gradient are magnified in these figures; the actual variations are quite small. Spike annealing shows a center to edge gradient with the highest APLU (10.3) in the center and 9.2 at the edge; flash annealing shows dark spots (8.1APLU) where the wafer lifters are located (an artifact of the earlier version of the tool used to process the wafers) compared to the other bright areas (7.7APLU); the SPE signature is slightly darker towards the center (35.9APLU) compared to the edge (32.4APLU); and laser annealing shows a step and repeat checkerboard pattern. Both full wafer PL imaging for macro-mapping and localized imaging for micro-mapping for another laser-annealed wafer with a scanning motion rather than a step and repeat motion revealing a spot size of ~5.5mm and 0.41mm of overlap is shown in Fig. 9. So PL analysis provides very good macro and micro sensitivity for mapping slight variations in non-uniformities.

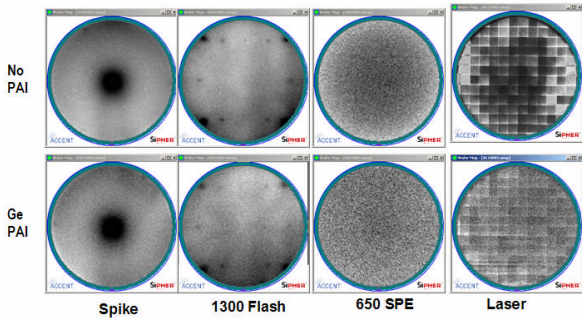

Fig. 8: PL full wafer map imaging of annealing signatures.

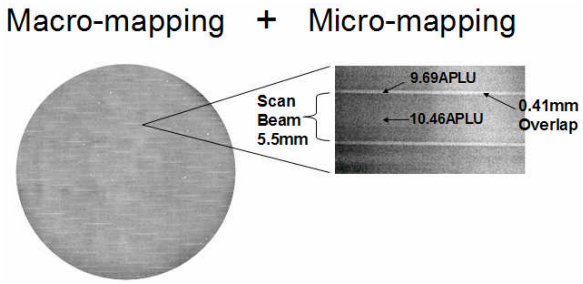

Fig. 9: Scanned laser beam annealing full wafer PL imaging showing macro and micro variations.

Junction quality/damage recovery was characterized by JPV R_sL leakage measurement. The results are shown in Table 3 (A/cm^2) and all the spike and Flash annealed samples – with or without Ge-PAI – had junction leakage <1E-7A/cm^2 (measurement sensitivity limit). As shown by X-TEM (Fig. 7c) and detected by PL (Table 2), the Ge-PAI wafers with laser annealing remained amorphous and the R_sL measured leakage was in the E-2 to E-3A/cm^2 range. While without PAI $B_{18}H_{22}$, $B_{10}H_{14}$ and B were in the 1–3E-7A/cm^2 range and BF_2 was 3E-6A/cm^2, which suggests residual EOR damage that was also detected by PL with an APLU of 27. Results for the SPE anneal showed that an excellent junction leakage current of 2E-7A/cm^2 measured for the $B_{10}H_{14}$ and $B_{18}H_{22}$ wafers suggests high quality junctions. The Ge-PAI wafers were in the E-5A/cm^2 level. The B and BF_2 wafers were in the E-5 and E-6A/cm^2 range, which also suggests EOR damage after SPE annealing and was also in agreement with the PL analysis results. X-TEM analysis of the SPE-annealed B wafer (Fig. 5b) clearly showed defects (not EOR damage) throughout the first 5.5nm in depth. Additional X-TEM analyses are scheduled in the future. Good correlation between R_sL junction leakage current to APLU was observed in Fig. 10.

Table 3. JPV junction leakage measurements (A/cm^2)

Dopant	Spike/1080	Spike/1000	Flash	Laser	SPE
B	1E-7	1E-7	1E-7	3E-7	1E-5
+PAI	1E-7	1E-7	1E-7	2E-2	6E-6
BF2	1E-7	1E-7	1E-7	3E-6	1E-6
+PAI	1E-7	1E-7	1E-7	1.5E-3	1E-5
B10-serial	1E-7	1E-7	1E-7	2E-7	2E-7
+PAI	1E-7	1E-7	1E-7	1.8E-3	3E-5
B10	1E-7	1E-7	1E-7	1E-7	2E-7
+PAI	1E-7	1E-7	1E-7	2.3E-2	3E-5
B18	1E-7	1E-7	1E-7	1E-7	2E-7
+PAI	1E-7	1E-7	1E-7	2.3E-2	2E-5

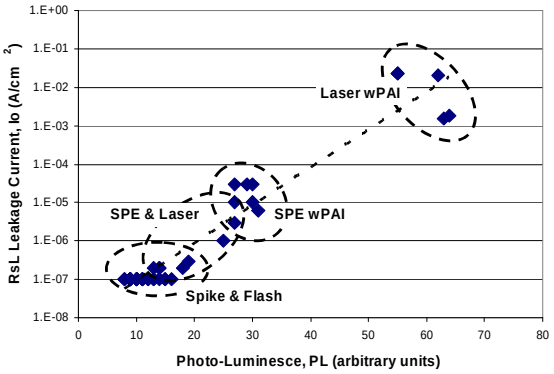

Fig. 10: Correlation of APLU to JPV leakage.

For shallow junctions <25nm deep, an accurate 4PP sheet resistance (R_s) measurement for dopant activation is very difficult to obtain due to probe penetration of any or all of the probes. Therefore, we compared several new alternative methods to measure R_s (ohms/square). Non-penetrating contact EM-4PP and Hg-4PP R_s results, as well as JPV R_s results are compared to standard 4PP with blunted probe tips and are shown in Table 4. For most of the conditions, good agreement between all the various R_s metrology techniques were verified, however, for some of the conditions, a wide range of R_s values were observed, especially for the B laser and SPE diffusion-less activation anneals even though SIMS analysis detected deep junctions of >24nm. The true electrical junction depth could be much shallower than the SIMS determined junction depth based on the B chemical (elemental) depth profile.

Table 4. Comparison of various Rs (ohms/sq.) metrology results (Hg/std/EM/JPV).

Dopant	Spike/1080	Flash	Laser	SPE
B	342/340/313/315	527/525/466/475	2200/2224/1209/1100	20403/19410/62K/7500
+PAI	349/340/342/315	538/512/473/470	no p/n	1227/1135/1235/1080
BF2	465/453/466/430	661/641/682/610	998/806/1378/996	4818/4856/4335/3600
+PAI	534/526/719/488	674/675/685/637	no p/n	2183/1746/2954/1872
B10-serial	590/579/535/536	905/895/831/791	844/988/857/706	2680/2676/2456/2175
+PAI	656/650/614/600	860/842/842/759	no p/n	1678/1025/1799/1488
B10	566/553/538/516	809/781/765/732	877/832/1494/511	2940/2961/3521/2377
+PAI	617/601/589/560	780/791/955/703	no p/n	3368/--/1531/1590
B18	405/393/378/368	539/526/503/484	583/580/561/728	1781/1785/1682/1493
+PAI	464/452/640/423	613/595/725/555	no p/n	1384/1099/1400/1239

From the R_s vs. X_j plot (Fig. 11), the dopant activation level was determined [5]; however, since there is always uncertainty in the true electrical junction depth, as well as the measured R_s value by each of these techniques, there is uncertainty in the true activated level. The determined dopant activation level also known as the boron solid solubility limit (B_{ss}) is listed in Table 3 [a) Nsurf and b) Bss derived from Rs-vs.-Xj]

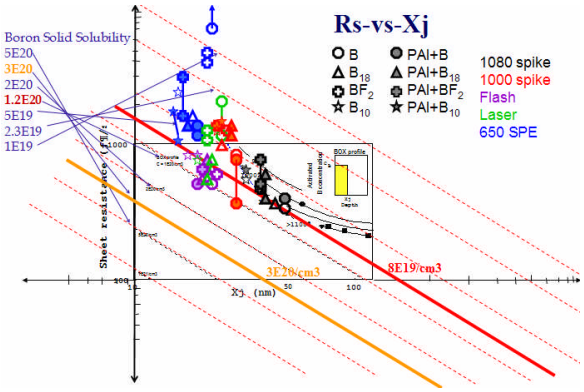

Fig. 11: Rs versus Xj for Bss dopant activation level determination.

Table 5: Carrier density /cm^3 determined by Nsurf or Bss (Rs/Xj)

Dopant		Spike/1080	Spike/1000	Flash	Laser	SPE
B	Nsurf	1.9E19	1.8E19	4.4E19	1.2E20	9E18
	Bss	7-8E19	5E19	1E20	2-4E19	<8E18
+PAI	Nsurf	5.5E19	7.2E19	9.5E19	no p/n	4.6E19
	Bss	7-8E19	5E19	9E19	no p/n	6E19
BF2	Nsurf	3.9E19	3.7E19	6.3E19	1.3E20	1.8E19
	Bss	8E19	3-4E19	8E19	4-7E19	1.5E19
+PAI	Nsurf	4.4E19	4.6E19	8.6E19	no p/n	1.4E19
	Bss	8E19	3-4E19	1E20	no p/n	3-4E19
B10-serial	Nsurf	4.8E19	6.3E19	9.2E19	1.6E20	7.4E19
	Bss	7E19	4E19	0.9-1E20	7-9E19	3-4E19
+PAI	Nsurf	4.2E19	5.2E19	8.9E19	no p/n	4.8E19
	Bss	7E19	3-4E19	8E19	no p/n	6E19
B18	Nsurf	4.2E19	4.7E19	9.7E19	1.4E20	6.3E19
	Bss	8E19	4-5E19	1.3E20	0.9-1.3E20	4E19
+PAI	Nsurf	5.2E19	5.3E19	1.2E20	no p/n	3.9E19
	Bss	7-8E19	3-4E19	0.9-1.2E20	no p/n	6E19

The wide spread in B_{ss} values for a specific annealing technique is due to the wide range in R_s values determined by the various metrology techniques listed in Table 4 and seen in Fig. 11. PAI+B with a 1000^{o}C spike anneal R_s determined B_{ss} varied from 0.5-1E20/cm^3 and PAI+BF_2 with SPE anneal B_{ss} varied from 2.5–5E19/cm^3. For this reason, a new technique to directly measure the near surface electrically active dopant density (Nsurf) within the top 3nm of the surface was developed using an EM-probe CV based technique. Using this technique, we could directly measure the surface activated dopant density, and therefore compare each implant species and annealing conditions without having to know the electrical junction depth.

Table 5 also shows Nsurf results. The highest Nsurf dopant activation levels were seen with laser annealing (1.6E20/cm^3) followed by flash (1.2E20/cm^3), and then spike annealing (7.5E19/cm^3), and SPE (7.4E19/cm^3) as shown in Fig. 12. For each annealing technique, the highest dopant activation was always detected for the molecular dopant species without Ge-PAI, while the opposite conclusion would be made using B_{ss} determined from the R_s vs. X_j data in Table 5. Except for the SPE annealing case, the B_{ss} values were similar,

with or without Ge-PAI for the spike and Flash anneals. For SPE anneals, the Ge-PAI wafers always had higher B_{ss} activated levels. For most of the cases good agreement was observed between Nsurf and Rs/Xj determined Bss as shown in Table 5. However, for some cases like the B spike annealed at both 1080°C and 1000°C the difference between Nsurf and Bss was as much as 4x (1.9E19/cm^3 versus 8E19/cm^3). The SIMS profile in Fig. 1a showed B diffusion at approximately 1.5E20/cm^3 with a surface pile-up of 2E21/cm^3 of electrically inactive B. Spreading resistance depth profile (SRP) was conducted on this sample by beveling and the result is shown in Fig. 13. A drop in the electrical active dopant level towards the surface is clearly observed by SRP in agreement with the lower Nsurf measurement shown in Table 5. Fig. 14 shows a plot of these Nsurf values versus SIMS measured Xj. For the B and BF_2 laser annealed cases the 6x lower activation Bss measurement compared to Nsurf could be explained if the true electrical junction depth was <8nm and not 26.8nm determined by SIMS. Additional beveling tests will be done to verify this.

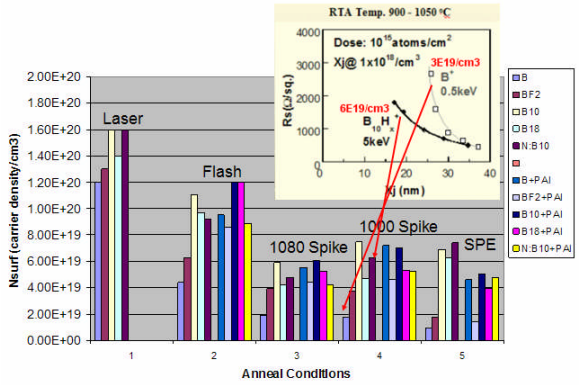

Fig. 12: Nsurf for various anneals.

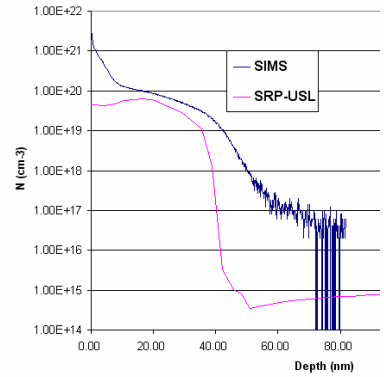

Fig. 13: SIMS versus SRP depth profile for B 1080°C spike annealing.

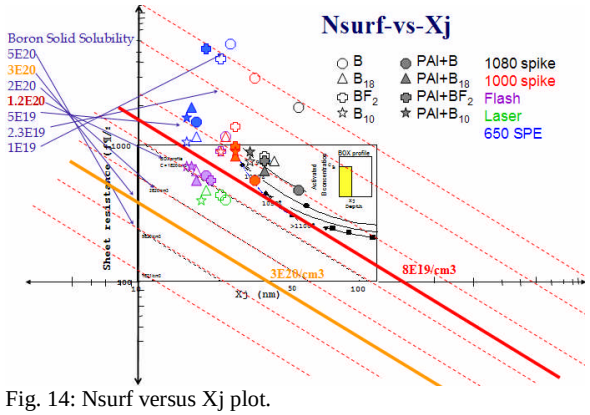

Fig. 14: Nsurf versus Xj plot.

4. Conclusion

High quality and high dopant activation p+ junctions ~15-20nm deep can be achieved using $B_{10}H_{14}$ or $B_{18}H_{22}$ with high temperature (>1300°C) flash or laser annealing, as well as low temperature SPE annealing at 650°C. These anneals enable the extension of beam-line implantation to beyond 32nm node with energies at 5–10keV. Therefore, molecular dopant species are very attractive for SiON gates using fast (msec) or ultra-fast (200nsec) annealing, or high-*k* Hf-oxide gates requiring low thermal budget processing.

Each advanced annealing technique for diffusion-less activation has a unique signature as revealed by PL wafer map imaging analysis that must be optimized for the best activated dopant uniformity. However, metrology to determine the activated dopant level for these diffusion-less techniques is still subjective and needs improved accuracy and repeatability, especially to determine the true electrical junction depth for the R_s vs. X_j plots. The Nsurf technique could provide this information in the future through beveling measurements.

5. References

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