

APPLYING IMPLANTATION EQUIVALENT SCALING TO GATE LENGTH SCALING BEYOND THE 90NM NODE

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We report on the results of using a single wafer multi-purpose implanter (MPI) to solve gate length scaling issues beyond the 90nm node. Use of molecular dopant species implantation such as $B_{10}H_{14}$, $B_{18}H_{22}$, As_2 and As_4 improves gate length (L_g) scaling and short channel effects (SCE) through HALO and source drain extension (SDE) implantation engineering. This is achieved by using a new ion source specifically designed for these heavy molecules. Precise uniform beam parallelism across a 300mm wafer for zero and high tilt angle implantation is critical in eliminating asymmetrical transistor effects caused by low energy beam divergence and wafer end-station angle variation effects seen on both batch and serial high current implanters, including energy contamination effects by avoiding low energy decel-mode of operation. High tilt SDE and PAI implantation for gate overlap control are also possible using molecular dopant species on medium current implanter adding process flexibility and creating a new classification called MPI (multi-purpose implanter).

INTRODUCTION

The last two decades the IC industry has been driven by the personal computer (PC) market with its ups and downs reaching about 185 million unit sales in 2004. The desktop PC uses high performance (HP) logic devices with high drive current and fast switching speed therefore requiring the highest scaling of gate length and ultra-shallow junctions (USJ) are key. Gate leakage is not so critical so SiON gates will be used through 45nm node since only a 40x reduction in gate leakage is required for 65nm node and 100x reduction at 45nm node compared to SiO_2 (1). This can be realized with a nitrogen content of >20% and a k value of >5 at 65nm node and a nitrogen content of >30% and a k value of >6 for the 45nm node. Portable note book PC uses high capacity batteries so lower leakage devices are required called low operating power (LOP) logic devices. For the first time starting in 2004 the mobile communication cell phone market is driving the IC industry with 640 million unit sales and consuming up to 31% of the worldwide semiconductors (2). Cell phones use low capacity batteries so these low standby power (LSTP) logic devices require low leakage to extend battery life. To achieve lowest junction leakage USJ requirements are relaxed but 3,000x reduction in gate leakage at 65nm node and 20,000x reduction at the 45nm node is required so Hf-based gate dielectric material will replace SiON gate dielectrics starting at the 65nm node using HfSiON with a k value between 9-11.

IMPLANTATION SOLUTIONS FOR GATE LENGTH (L_g) SCALING

At the 65nm node L_g will be <32nm in length with a gate stack poly height of <85nm. To continue gate scaling and improve short channel effects (SCE) both the HALO and SDE implanted structure must also be scaled. To minimize HALO overlap under the channel preventing mobility degradation, high tilt HALO implantation energy is decreasing while the dose is increasing as reported by Shahidi and illustrated in Fig. 1 (3). With diffusionless activation the precision of the HALO structure becomes very critical so angle

and dose control is extremely important. However, spike/RTA will still be used at the 65nm node since flash/RTA, non-melt laser annealing and SPE annealing methods are still not mature so there will be some amount of dopant movement/diffusion. Minimizing L_g is limited to SCE and V_t roll-off which is influenced by HALO and SDE lateral dopant interaction.

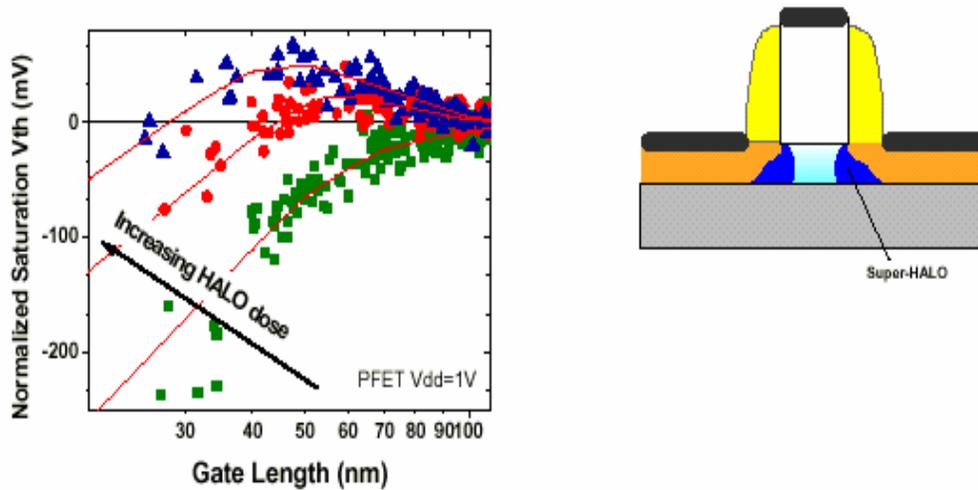


Fig. 1: Interaction of HALO and SDE implants on V_t roll-off and L_g scaling (3).

HALO SCALING

The precision and uniformity of HALO dopant placement becomes more critical with scaling. As gate stack spacing decreases, high aspect gate stacks suffer from shadowing therefore requiring lower tilt angles going from 45 degrees down to 30 degrees avoiding all the preferred channeling tilt angles at 36.7, 35.3, 33.7 and 26.6 degrees (4). With decreasing L_g and increasing HALO dose, the HALO structure will overlap (5) leading to the HALO doping directly affecting the channel doping concentration resulting in impurity scattering and channel mobility degradation as reported by Ghani et al. and shown in Fig. 2 (6). One solution is to reduce the HALO implant energy thereby reducing also the dopant lateral straggle and HALO overlap. However lower implantation energies leads to increased beam divergence (blow-up) and reduction in beam current (implanter productivity). Therefore the best solution is to go to higher mass dopant species allowing for higher implantation energies using BF_2 , In, $B_{10}H_{14}$ or $B_{18}H_{22}$ for p-type species and Sb, As_2 or As_4 for n-type species. Umisedo et al. reported that at the same equivalent low energy boron HALO at 5keV, $B_{10}H_{14}$ reduced beam divergence angle by 12x from 1.2 degrees to 0.10 degree and beam size by 11.4x from 139mm to 12mm (7). Ito et al., reported steep retrograde surface profiles using In HALO with flash/RTA maintaining a surface dopant level $<1E15/cm^3$ while with spike/RTA it went up to $3E17/cm^3$ (8). Also, using the higher mass dopant species such as In and Sb have been reported to result in amorphization which prevented channeling of the subsequent SDE implant.

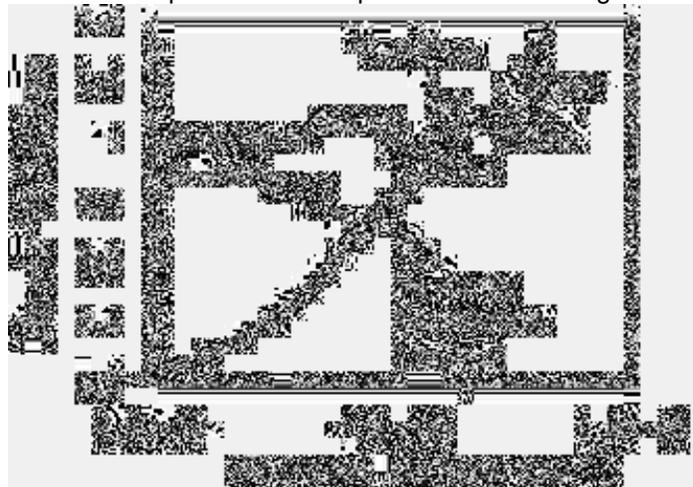


Fig. 2: Effect of HALO and therefore channel doping level on mobility degradation (6).

SDE SCALING

The other aspect of Lg scaling is SDE ultra-shallow junction (USJ) formation. A 500eV boron implantation into a PAI (pre-amorphization implant) structure is required to achieve the 14nm junction depth target of the 65nm node without channeling using diffusionless activation annealing as shown in Fig. 3. With spike/RTA annealing at 1080°C up to 15nm of boron diffusion will occur so < 100eV implant would be needed (9). At such a low energy for improved productivity decel mode implantation would be required, however, energy contamination (EC) gets worse at lower energies and with Lg scaling devices become more sensitive to EC so drift mode is preferred. Typically 0.03-0.1% EC is required depending on specific product type. At 200eV a 10 to 1 decel ratio results in 1-2% EC, at 5 to 1 ratio about <0.5% EC, at 3 to 1 <0.3% EC and at 2 to 1 <0.1% EC. The productivity drops-off to <5wph at a decel ratio of 2 to 1 at 200eV as shown in Fig. 4 making it impractical to use atomic B any longer. The channel doping level range for 65nm node HP logic is $2.5\text{-}5\text{E}18/\text{cm}^3$ and for LOP & LSTP logic it is in the $0.8\text{-}2\text{E}18/\text{cm}^3$ range making them very sensitive to small amounts of energy contamination(1).

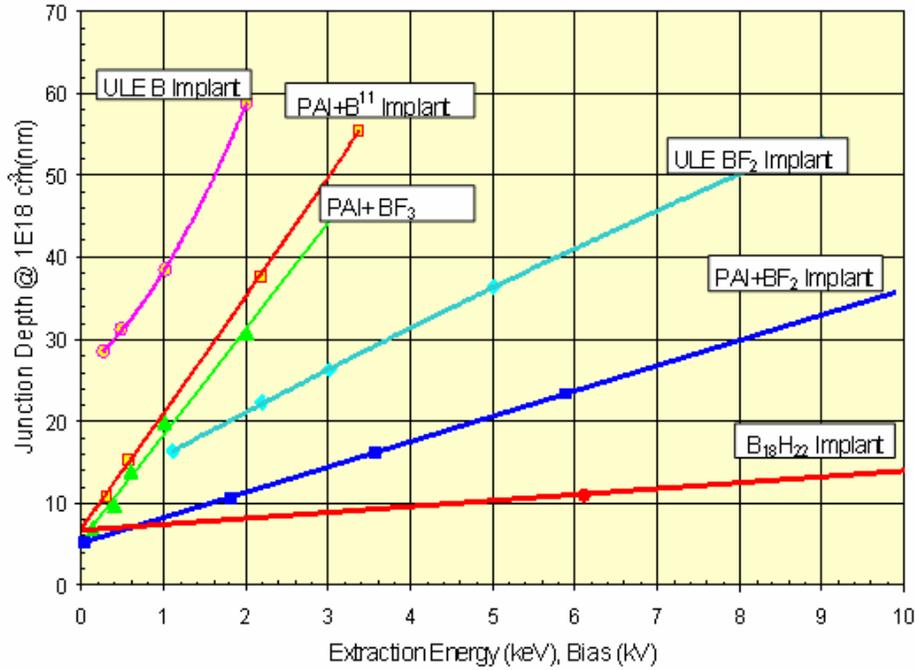


Fig. 3: Boron implant energy versus Xj.

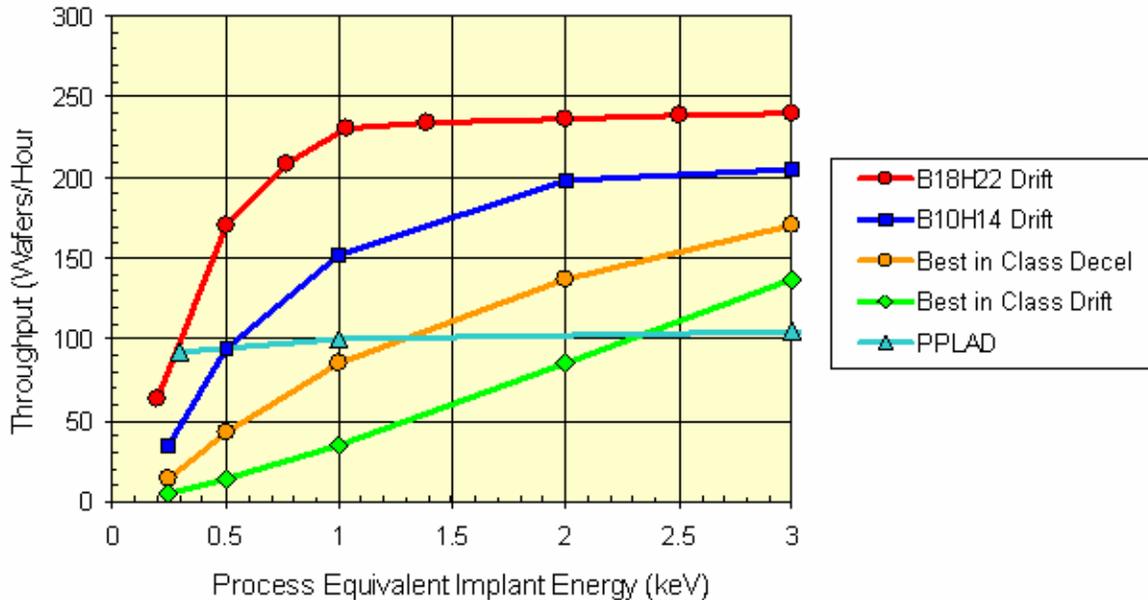


Fig. 4: 300mm throughput numbers for 200eV to 3keV equivalent boron implant energies at 1E15/cm² dose.

IMPLANTATION EQUIPMENT ISSUES (DESIGN & IMPLANT SPECIES)

Starting at the 90nm node, batch end-station designs for high energy and high current ion implanters have become problematic due to the cone angle effects which are directly limiting device isolation and transistor gate length (L_g) scaling. To extend batch end-station new designs to reduce the angle variation across a 300mm wafer is required. Kawasaki et al reported on the results from going from a 5 degree cone angle disk to a 2 degree disk for batch high energy implantation to reduce the cone angle effect but not totally eliminate it (10). Similarly, Wan et al. reported on improvements in going to a specially designed wafer pad for their batch high current implanter and this reduced the cone angle effect from 1.2 degrees down to <0.2 degree (11). However, to totally eliminate this effect requires single wafer ion implanters with spot scanned beam with 1-D mechanical scan to realize parallel beam. Modifying the Nissin Exceed medium current implanter with a molecular dopant species ion source that solves the gate length scaling limitations created by non-parallel beam observed with batch end-station design and both broad beam with 1-D mechanical scanning and spot beam with 2-D mechanical scanning serial end-station designs as will be described below in Figs. 5 & 6.

The SDE implant is typically done at zero tilt however, with the move to diffusion-less activation any variation to the precision of the implant across the wafer shows up directly as variations in device electrical results due to the formation of asymmetrical transistors as reported by Yoneda and Niwayama in Fig. 5 (12). Three detrimental effects on L_g scaling has been reportedly caused by batch high current end-station designs. First, similar to what was described above for the HALOs, beam blow-up effects has now become evident starting with arsenic nSDE implantation at the 130nm and 90nm node since very little diffusion occurs with spike/RTA annealing. With boron there still is about 15nm of diffusion so beam blow-up effects are not sensitive to asymmetrical pSDE. For narrow gate stack to gate stack spacing, SDE dose loss to the sidewall of the gate stack structure is observed due to beam blow-up. Using higher mass dopant implant species such as As_2 , As_4 , $B_{10}H_{14}$ and $B_{18}H_{22}$ reduces beam blow-up as mentioned in the HALO section earlier and reported by Umisedo et al. (7). The second detrimental effect is again asymmetrical transistors caused by the batch end-station cone angle effects causing ± 1 degree tilt angle variation across the wafer as shown in Fig. 5 due to the gate stack poly structure shadowing effects. Elzer & Sing measured the batch high current cone angle effect using thermawave (TW) analysis as shown in Fig. 6a (13). This effect is reduced using a ribbon beam with 1-D mechanical scanning as reported by Bertuch et al. shown in Fig. 6b but vertical stripping is still evident (14). To eliminate this effect requires a spot scanned beam with 1-D mechanical scanning as shown by the TW result in Fig. 6c. The third effect is unique to wafers subjected to high lateral speeds and momentum like on a spinning disk which can cause catastrophic gate stack poly structure failure as reported by Kawasaki et al and shown in Fig. 7 a & b (15). As L_g is scaled to below 100nm as shown in Fig. 7a, particles traveling down the beam line would impact the wafer and the high speed spinning disk directional momentum. This causes the gate stack poly line to collide with the particle resulting in the poly gate line breakage as shown in Fig. 7b. The solution is to maintain extremely clean particle free beamline with a batch end-station and reduce spin speed from 1200 rpm to <300 rpm or to use a single wafer end-station with no significant directional momentum of the wafer.

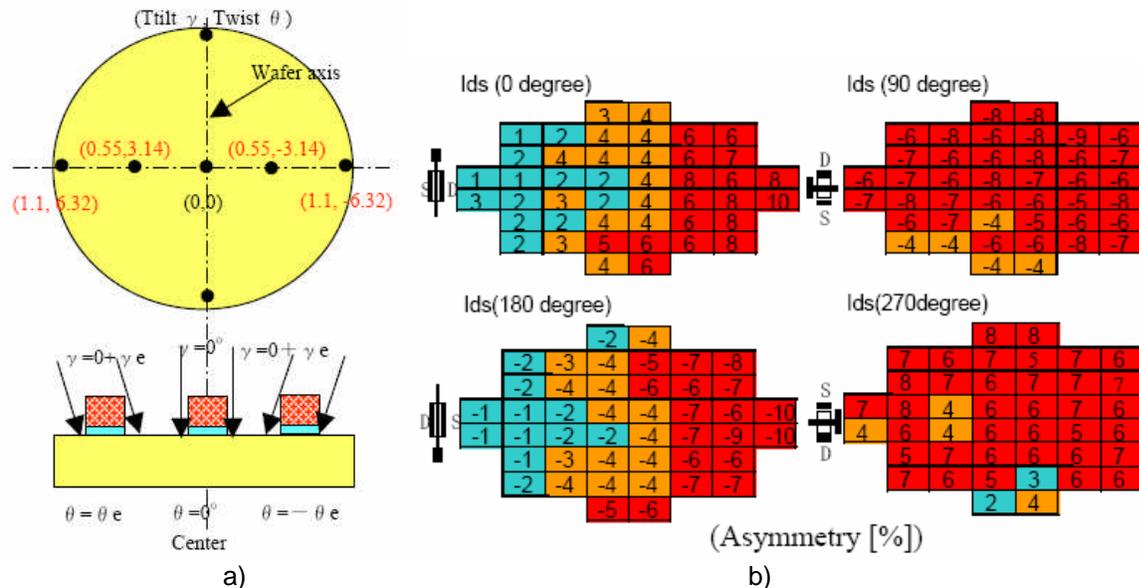


Fig. 5: Batch end-station cone angle effects on gate stack shadowing of SDE implant resulting in asymmetrical nMOS transistor characteristics (12).

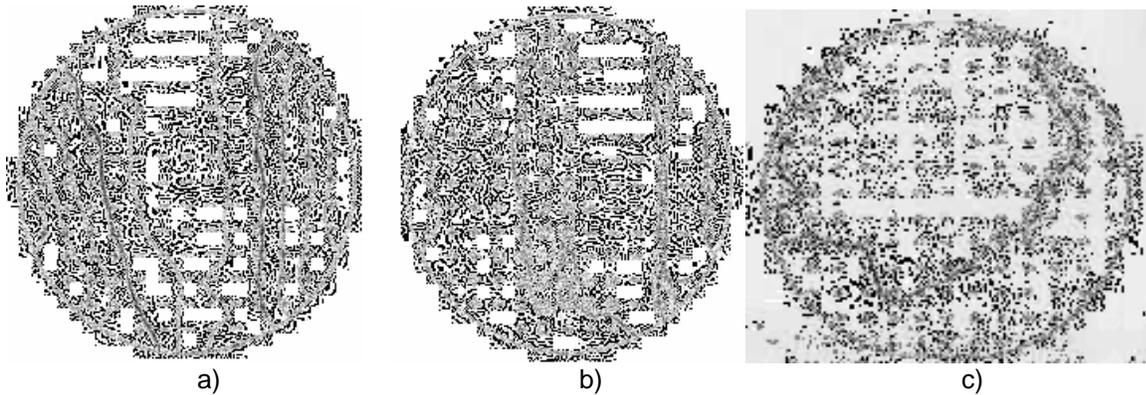


Fig. 6: Thermawave wafer uniformity mapping results at zero tilt angle for: a) batch high current showing cone angle effects (13), b) serial ribbon beam high current (14) and c) serial spot scanned beam.

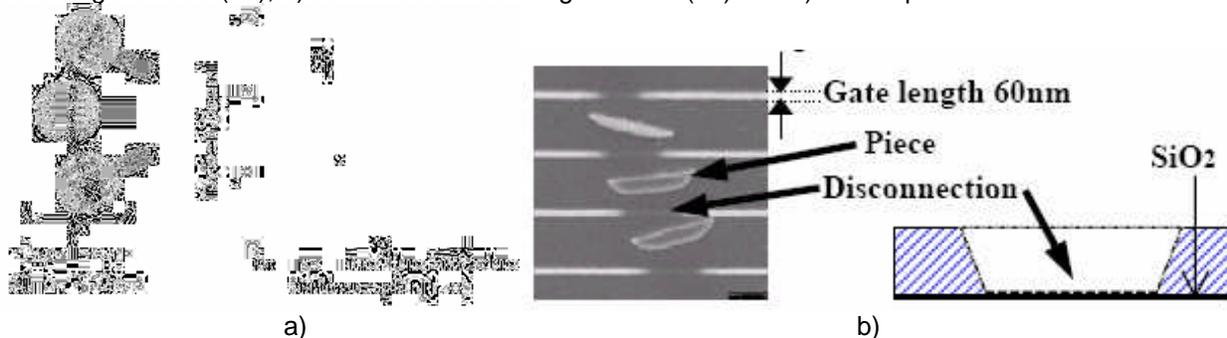


Fig. 7: High current beam line particle and spinning disk effects in causing gate stack poly failure (15).

Another issue with Lg scaling is SDE gate overlap control. As lateral diffusion is reduced, implant dopant lateral straggle is no longer sufficient to achieve the desired lateral gate overlap. Therefore both tilted SDE and PAI implantation up to 30 degrees will be necessary to achieve a 0.5x lateral overlap as reported by Borland et al., Lindsay et al. and Thirupapulipur et al. (5,16,17).

Using $B_{10}H_{14}$ as a p-type dopant alternative for boron also results in a 10x increase in equivalent beam current while $B_{18}H_{22}$ results in a 18x increase. Up to 10mA effective beam current can be realized at 500eV as shown in Fig. 8. Fig. 9 compares thermawave results of atomic B to $B_{10}H_{14}$ (18). Note the 2x higher TW units of 1600 for $B_{10}H_{14}$ at a dose of $1E15/cm^2$ compared to 800 TW units for atomic B suggesting significant more silicon damage with the molecular dopant species. Another benefit of using $B_{10}H_{14}$ is the non-channeling as-implanted boron SIMS profile shown in Fig. 10 suggesting self-amorphization due to the large molecular dopant size and the higher TW unit measured in Fig. 9. X-TEM analysis of $B_{10}H_{14}$ showing the presence of a thin surface amorphous layer can be seen in Fig. 11. This would also eliminate the need for PAI implantation used to eliminate boron channeling for USJ and thereby avoid an additional high current implant step. Results for a 200eV boron equivalent implant using $B_{18}H_{22}$ at 4keV is shown in Fig. 12 and 5nm of reduced channeling is clearly seen. Molecular dopant species implantation extends medium current implantation application space into the low energy high current space as illustrated in Fig. 13 and enables high tilt SDE and PAI. The impact of using $B_{18}H_{22}$ and the increased implanter productivity on high current implanters is illustrated in Fig. 14 and the dramatic effect it has on reducing the number of high current implanters needed per fab 300mm by up to 6x.

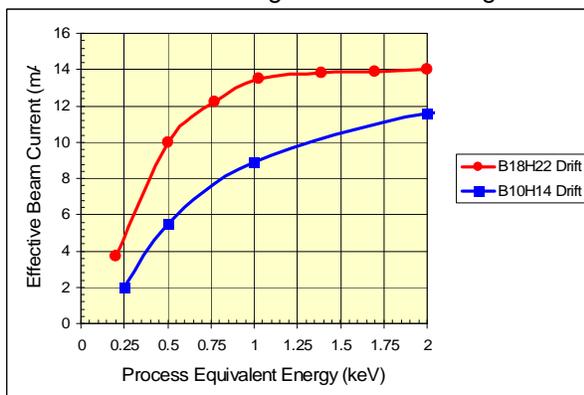


Fig. 8: Effective beam current comparison for $B_{10}H_{14}$ and $B_{18}H_{22}$.

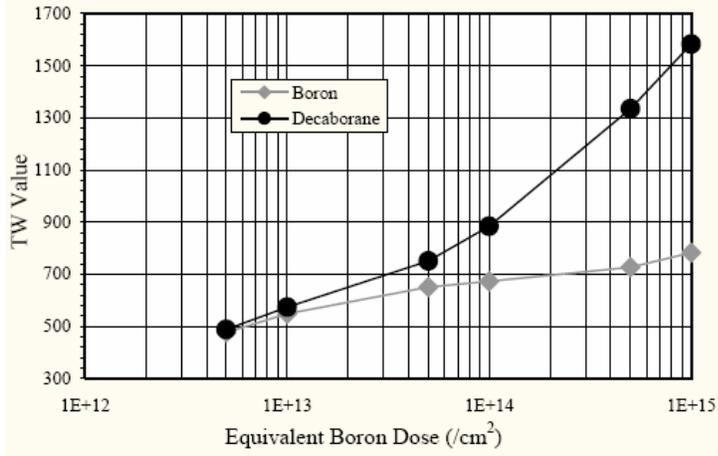


Fig. 9: TW comparison for atomic B and $\text{B}_{10}\text{H}_{14}$.

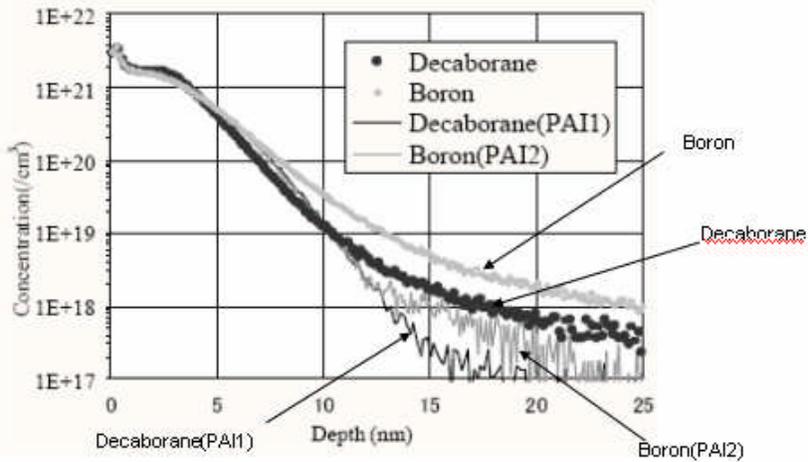


Fig. 10: SIMS comparison for a 500eV implant into crystalline silicon and PAI.

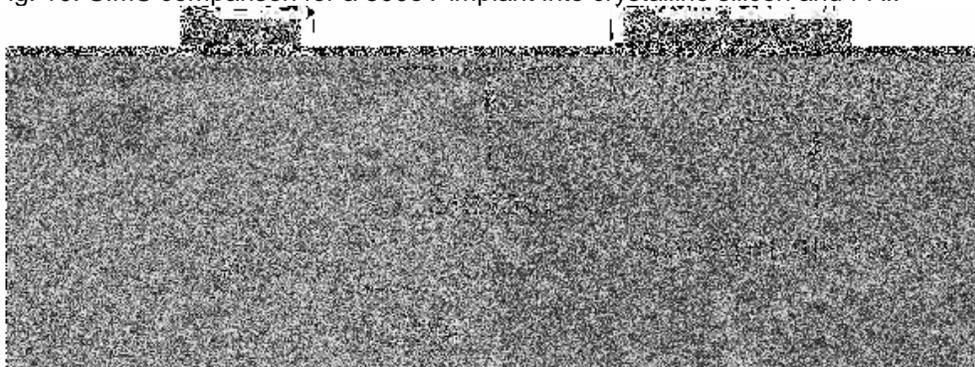


Fig. 11: X-TEM showing surface amorphous layer.

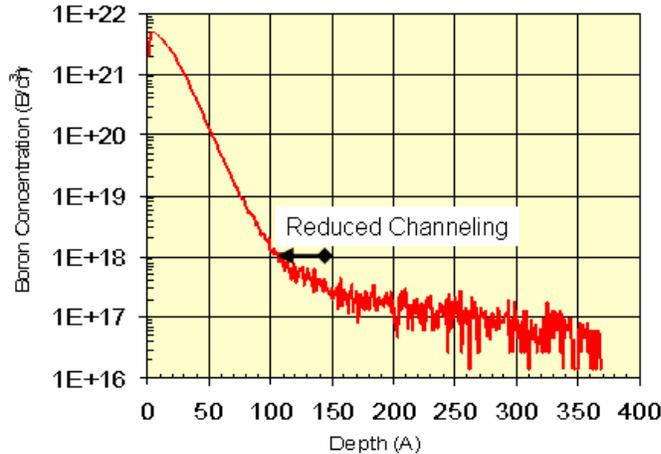


Fig. 12: Reduced channeling using $\text{B}_{18}\text{H}_{22}$ for a 200eV equivalent implant.

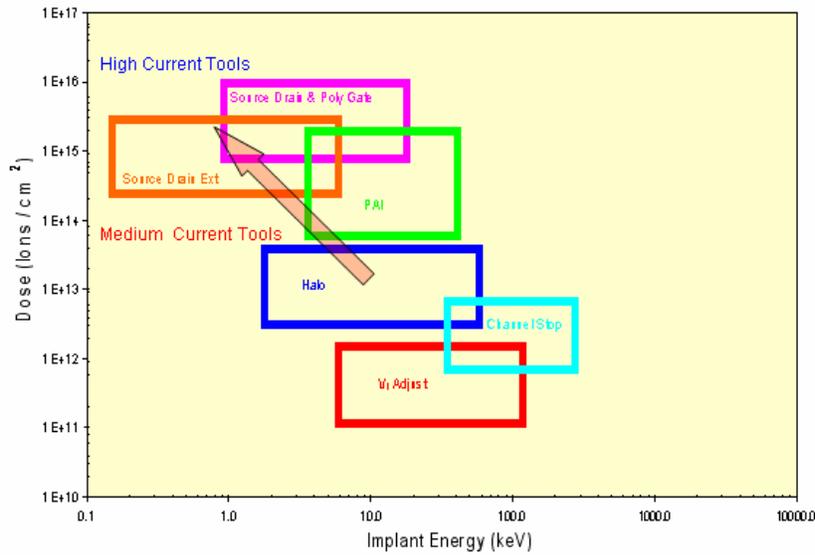


Fig. 13: Use of molecular species dopant implantation to extend both medium and high current application space.

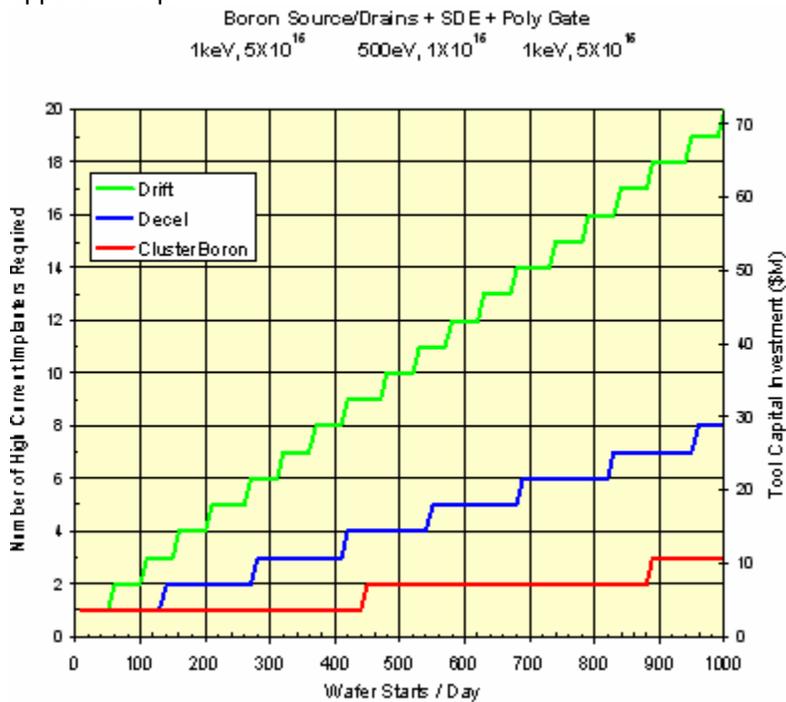


Fig. 14: Up to 6x reduction in the number of high current implanters when implementing molecular species dopant implantation.

ACTIVATION

One of the major issue with implementing any of the 3 diffusion-less activation methods (flash/RTA annealing, laser non-melt annealing or low temperature SPE annealing) is the issue of junction leakage degradation due to the residual end-of-range (EOR) from the PAI implant after annealing which has been reported to be as much as 3 orders of magnitude as shown in Fig. 15 (19). The reduced channeling and self-amorphization characteristics of large molecular dopant species such as B₁₀H₁₄ and B₁₈H₂₂ without residual EOR damage could be the breakthrough needed to make advanced diffusionless activation production worthy enabling excellent junction leakage current with excellent dopant activation and low sheet resistance.

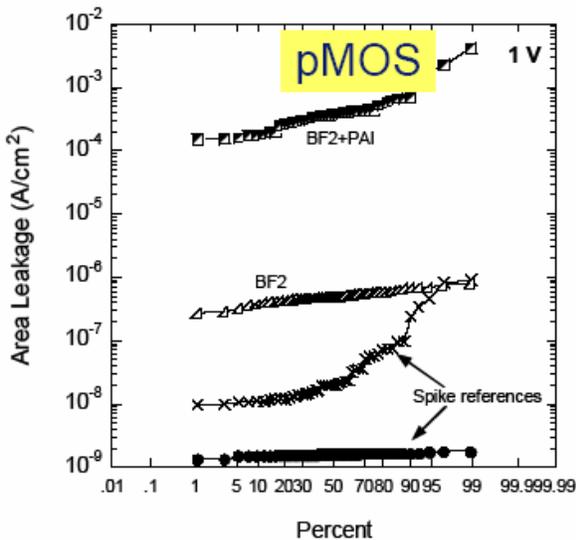


Fig. 15: Flash/RTA junction leakage results comparing with and without PAI (19).

SUMMARY

Use of molecular dopant species implantation such as $B_{10}H_{14}$, $B_{18}H_{22}$, As_2 and As_4 improves gate length (L_g) scaling and short channel effects (SCE) through HALO and source drain extension (SDE) implantation engineering. The heavy molecular dopant species significantly improves the implanter throughput at low energies without energy contamination in drift mode and induces self-amorphization eliminating the need for a separate PAI implant. The elimination of EOR damage should also improve junction leakage especially for diffusionless activation annealing. When implemented on a medium current implanter high tilt implantation down to 200eV is achieved for precise SDE gate overlap control. This also eliminates asymmetrical transistor formation and gate stack failure observed with batch end-station and some single wafer end-station designs.

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