Accurate Determination Of Ultra-Shallow Junction Sheet Resistance With A Non-Penetrating Four Point Probe

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Abstract

An accurate method to measure the four point probe (4pp) sheet resistance (R_s) of USJ Source-Drain structures is described. The new method utilizes Elastic Material gate (EM-gate) probes to form non-penetrating contacts to the silicon surface. The probe design is kinematic and the force controlled to ensure elastic deformation of the probe material. The probe material is selected so that large direct tunneling (DT) currents can flow through the native oxide thereby forming a low impedance contact. In this paper, the new 4pp will be demonstrated on a variety of implanted USJ structures

1. Introduction

To produce Ultra-Shallow Junction (USJ) structures careful process design of the pre-amorphization implant, S/D implant and the dopant activation and implant anneal are required. The USJ junction depths and level of dopant activation depend heavily on processing [1]. A suitable method for characterizing these USJ structures is the conventional four point probe (4pp) sheet resistance (R_S) technique [2,3]. The measured R_S is highly sensitive to the activated carrier density and x_j. This is a highly accurate, absolute method that has been used successfully on structures with deeper junction depths and layer thicknesses. Conventional 4pp R_S measurements generally use four penetrating, scrubbing probes placed in contact with the top layer of the semiconductor wafer. It is necessary for conventional 4pp probes to penetrate through any existing native oxide on the semiconductor surface in order to make good electrical contact to the top semiconductor layer. A common problem that now exists in the industry is the conventional 4pp method penetrates through USJ S/D structure into the semiconductor substrate. Under these circumstances, the R_S of the underlying substrate is measured. Generally this results in low R_S values and all sensitivity to the top USJ layer is lost.

In this paper, a new technique is presented that uses non-penetrating, non-damaging Elastic Material gate (EM-gate) probes to make accurate and repeatable 4pp R_S measurements on USJ S/D structures. There is no fundamental limit of this technique on USJ x_j. Layers as thin as 15 nm have been measured and will be presented.

2. Conventional 4pp Basics and Theory

A description of a conventional 4pp is shown in Fig.1.

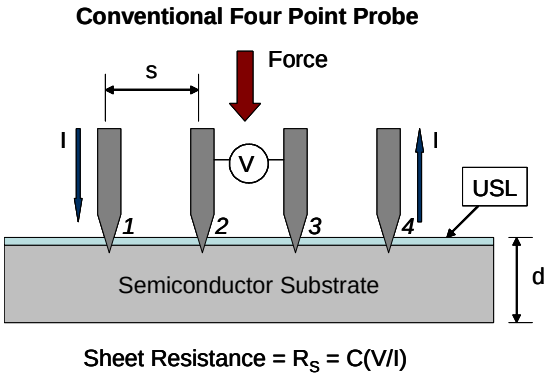

Fig.1: Schematic of a conventional 4pp setup. C is a geometric correction factor.

The probes are generally conditioned to be penetrating so that any top native oxide can be compromised and a good electrical contact to the top surface of the semiconductor made. This methodology works well for 4pp measurements on bulk or thicker layer structures. However, as shown in the results section, conventional 4pp measurements produce invalid data for the case of USL structures. Additionally, the probes are not kinematically mounted so that probe scrubbing occurs. This results in damage to the semiconductor surface and can also lead to changes in probe spacing, s, from measurement to measurement.

The credibility of 4pp measurements is usually established by measuring a NIST traceable reference standard to ensure accuracy of the probes, corrections, IV instrumentation, etc.. Also, during the measurement, some simple checks are made to ensure the quality of each measurement. These

checks include a current polarity reversal check and a half tolerance current check. The reverse current test checks the V/I measured with equal but opposite polarity currents and the half tolerance test checks the V/I at full and half current levels. These checks are valuable for detecting measurement errors due to surface and probe related effects.

3. EM-gate 4pp Description and Theory

The conventional 4pp measurement relied upon penetrating probes to make good electrical contact to the doped semiconductor surface. The use of conventional 4pp measurements on sub-50nm USJ structures can produce erroneous results. The actual limit and amount of probe penetration depends on the probe design and conditioning and, the probe load. Generally loads of about 100 gm are used. EM-gate 4pp measurements overcome all of the problems associated with conventional 4pp systems by using the same non-penetrating, non-damaging probes used to measure ultra-thin gate dielectrics(<1.0nm) [4]. A close-up illustration depicting the major mechanical differences between the probes is given in Fig.2.

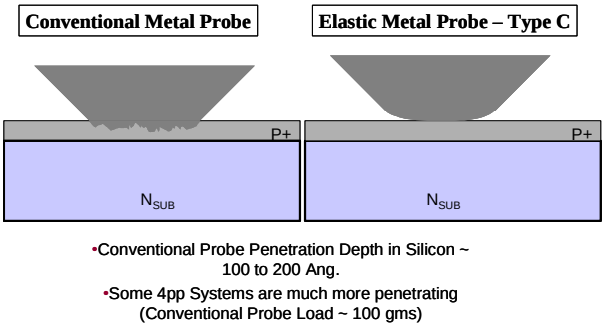

Fig.2: Penetrating versus non-penetrating 4pp designs.

From the substrate physics point of view, all of the formulae for calculating sheet resistance or resistivity are the same. There are some distinct differences in the equivalent circuit for the EM-gate 4pp. Unlike the conventional 4pp system where electrical contact is made via probe penetration and scrubbing, the EM-gate 4pp setup relies upon DT transport through the thin native oxide present on a semiconductor surface. Current transport by DT is limited to the case where the oxide physical thickness is less than about 4.0nm. This is generally the case for native oxides. Additionally, an applied voltage of at least about 0.5 V between the current carrying probes is required. This is also generally the case for 4pp measurements.

DT currents are observed for oxide thicknesses of 4.0nm and less. In this mode, DT and soft breakdown occurs. These processes are non-damaging and reversible. For the case of thicker oxides (>5.0nm), indirect tunneling and hard breakdown occurs. Even though the post hard breakdown current level can easily reach 1mA, implying a low resistance contact hard breakdown processes are undesirable since they can locally damage both the probe and wafer site. The EM-gate 4pp system operates in the DT mode, which means that the surface oxide should not exceed 4.0nm.

The potential is measured with a Kelvin-type setup where the input impedance of the voltmeter is high (~1E14 ohms). This means, in principle that no current loop exists between the voltage sensing probes. The measured potential is confined to the region where the current flows which is in the substrate. So considering voltage sensing, no tunneling is required through the surface oxide. Only for the two current carrying probes are DT current flows necessary for the measurements. During normal operation, EM-gate 4pp measurements are operated in the fixed current mode. Typically for USJ S/D structures, a current of 1mA is applied.

4. Results and Discussion

A highly useful and informative plot that describes the relationship between R_S, x_j and annealing processes for USJ S/D structures is shown in Fig.3. This plot is based on a significant amount of experimental data gathered from multiple processes

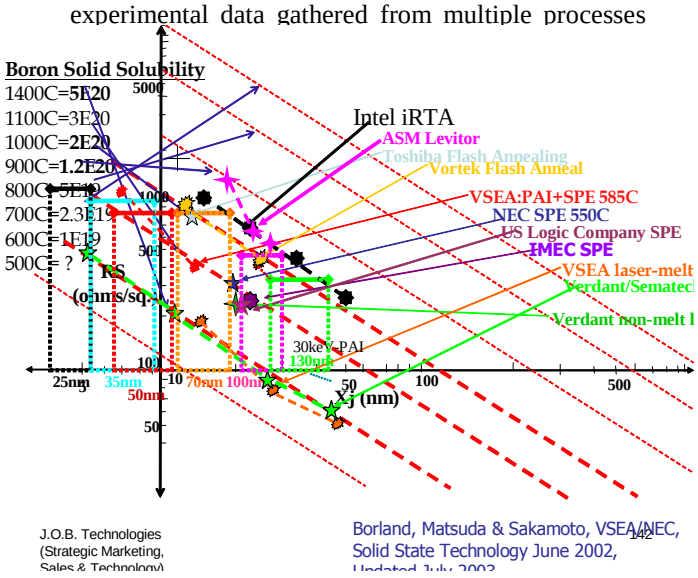

Fig.3: Plot of R_S versus x_j for common annealing processes.

Several cases are presented of EM-gate 4pp measurements on USJ S/D structures. Case 1 is for N+/P junctions and case 2 is for P+/N junctions.

A.Case 1

Arsenic implanted USJ S/D structures were evaluated with the EM-gate 4pp. The junction depths determined from both SIMS and SRP are about 30nm [2,6]. The SIMS chemical profile and SRP carrier density profiles are shown in Figs. 4 & 5 respectively.

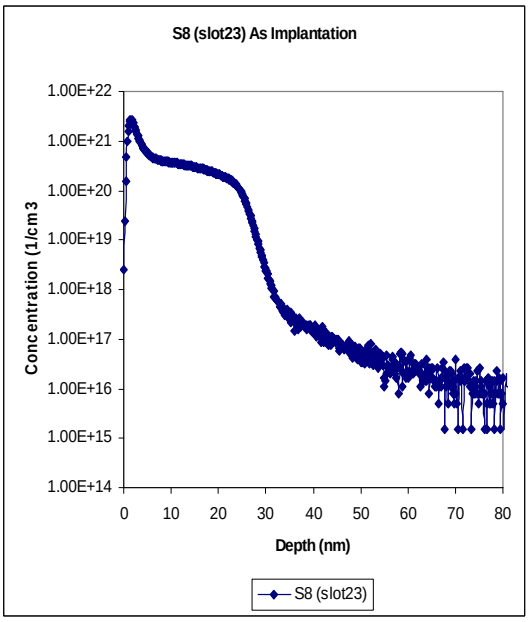

Fig.4: SIMS profile for Arsenic Implanted USJ S/D structures.

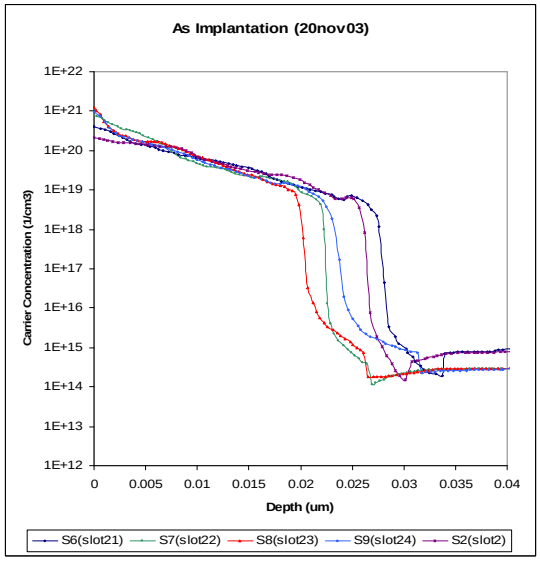

Fig.5: SRP profiles for arsenic implanted USJ S/D structures.

The sheet resistance was measured by various techniques for comparison including advanced 4pp, EM-gate 4pp, Variable Probe Spacing (VPS) method and SRP [6]. The advanced 4pp measurements were made with a kinematic, non-scrubbing 4ppwith a probe load of 45 grams. This type of 4pp is less penetrating and less damaging compared to standard 4pp systems. All of the Rs results obtained are summarized in Table 1.

Wafer	Backside Rs	Advanced 4pp Rs	EM-Gate 4pp Rs	VPS Rs	SRP Rs
Slot 2	122.9	237.1	288.5	300.6	290.9

Table 1: Advanced, EM-gate, VPS and SRP R_S measurements on Arsenic Implanted USJ structures with Xj_j = 30nm.

The advanced 4pp measurements yielded lower sheet resistances due to probe penetration into the top USJ S/D structure. A line plot comparison of all of the R_S measurements is given in Fig. 6. An ASTM-F84 ten point map was made with each measurement method.

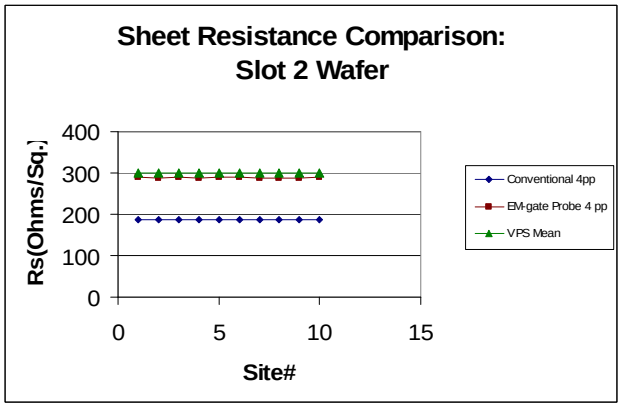

Figure 6: Sheet resistance comparison for ASTM F84 ten point maps made by conventional 4pp, EM-gate 4pp and the VPS methods.

B.Case 2

EM-gate 4pp R_S measurements were made on P+/N USJ S/D structures. Also sheet resistance measurements were made with a conventional 4pp. Histogram comparisons of the EM-gate and conventional 4pp results are shown in Figs. 7 to 9 for the 550°C, 750°C and 950°C 1 hour anneals.

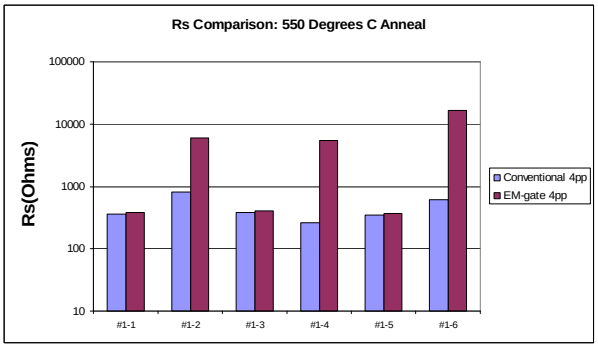

Fig.7: EM-gate versus Conventional 4pp R_S comparison for the samples annealed at 550°C.

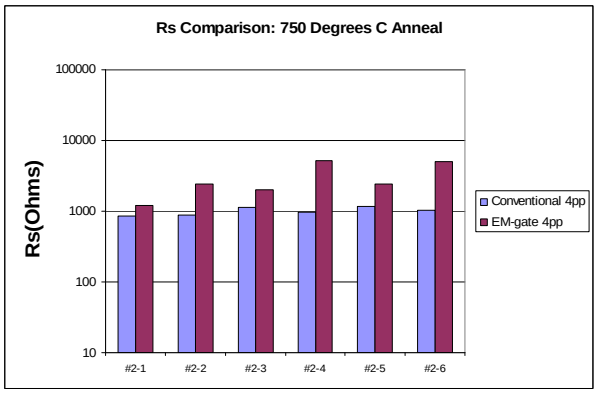

Fig. 8: EM-gate and conventional 4pp measurements for the samples that received a 750°C anneal.

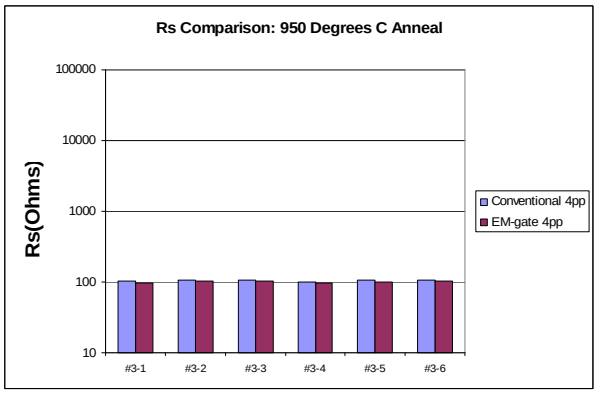

Fig. 9: EM-gate and conventional 4pp measurements for the samples that received a 950°C anneal.

The EM-gate R_S values for the amorphous implanted SPE wafers are lower, as expected, due to higher activation. The non-amorphous wafers have higher R_S values due to lower activation. The values obtained from the EM-gate 4pp are consistent with expectations and are in agreement with those predicted from Fig.3.

From SIMS and SRP depth profiles, the 950°C annealed samples have the deepest junction depths; 350-380nm. The shallowest x_j's are around 15nm measured by SIMS for the 550°C anneals and 0-17nm by SRP. From the SIMS junction depths and the measured R_S values, it can be concluded that the EM-gate 4pp can credibly measure USJ S/D structures with junction depths of 15nm determined by SIMS chemical dopant depth profiling. From the gate dielectric data presented earlier in this paper, it is likely that EM-gate 4pp can measure junctions significantly shallower (<1nm) if required. Again, the conventional 4pp seems to be limited to structures with junctions >35nm deep as mentioned in case 1 above.

5. Summary

EM-gate 4pp R_S measurements were described and several cases were presented; one for USJ P+/N and one for N+/P USJ S/D structures. It was found that the EM-gate 4pp could measure S/D structures with junction depths of 15nm. Conventional 4pp were found to be limited to about 30-40nm and deeper junctions. The three day repeatability of EM-gate 4pp R_S was found to be better than 1%.

6. Acknowledgements

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7. References

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