USJ Formation & Characterization For 65nm Node and Beyond

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Abstract

Multiple new methods of forming ultra-shallow junctions (USJ) are being pursued for 65nm node based on; 1) new ion implantation hardware designs, 2) new cluster ion dopant species, 3) new zero diffusion dopant activation annealing equipment and 4) non-implantation alternative selective epi in-situ doping techniques. Also, improved accurate measurement and characterization techniques to determine the electrically active dopant level and depth profile as opposed to the chemical (electrically inactive) dopant level and profiles are being developed.

1. Introduction

Starting at the 65nm node the industry will migrate to diffusion-less (zero diffusion) activation with SDE (source drain extension) junction depths in the 13-30nm range depending on device application. High performance (HP) logic devices drives the shallowest junction with lowest Rs while low operating power (LOP) and low standby power (LSTP) logic devices allows deeper diffused junctions with lower leakage requirements. With diffusion-less activation by Flash/RTA, laser spike anneal (LSA) or low temperature SPE, high tilt implantation for PAI (pre-amorphizing implant) and SDE implants up to 35 degrees are being investigated for 65nm node to achieve the desired gate overlap control and dopant activation laterally under the gate edge (up to 15 degree tilted implantation is already used at the 90nm node) [1]. These shallower junctions in the 10-20nm range require improved non-penetrating 4-point probe (4PP) measurement methods for Rs measurements. SIMS measurement is also reaching it's limit since the chemical dopant profile is no longer representative of the electrical dopant profile due to dopant solid solubility limit in silicon and enhanced electrical activation by engineering the PAI location. This difference between chemical inactive concentration to electrical active concentration can be one to two orders of magnitude. Therefore, this paper will review the current options being considered for USJ formation including: 1) implant/doping roadmap (Fig.1), 2) dopant activation/annealing roadmap (Fig.2) and 3) junction measurement & characterization roadmap (Fig.3).

2. Implantation /Doping Roadmap

Presently the lowest implant energy used in production at the 90nm node is B_{11} at 500eV for pSDE. With an implant dose of 1E15/cm^2 the as-implanted junction depth (Xj) defined at 1E18/cm^3 by SIMS is approximately 21nm due to channeling while with PAI to eliminate channeling it is 12nm. The 65nm node target of 14nm would require PAI with 500eV B_{11}. In drift mode the best in class high current implanter would have a throughput of <15 wafers/hour (300mm) at a dose of 1E15/cm^2 [2]. Running in decel-mode would increase throughput up to 49wafers/hour (300mm) but at the expense of significant energy contamination. Therefore, the key with using sub-keV B_{11} implantation energies is minimizing decel-mode energy contamination to <0.035-0.25% depending on the uniform channel doping level as defined in the ITRS-2003 roadmap [3]. For HP logic the channel doping level at the 65nm node will be 2-5E18/cm^3 while LSTP logic will be 0.7-2E18/cm^3. To eliminate line-of-sight energy contamination Chen of AIBT reported designing an "S-bend" in their iStar implanter beam-line to guarantee energy contamination control to <0.1% [4]. Otherwise, to improve productivity without energy contamination would require switching to another boron dopant species.

Switching from B_{11} to BF_2 allows 5x increase in implantation energy going from 500eV B_{11} to 2.5keV BF_2 and still maintain an as-implanted Xj of 12nm with PAI and 62wph throughputs [5]. However, there have been technical reports on lower boron dopant activation with BF_2 compared to B_{11} for pSDE. For this reason several companies are now evaluating boron cluster ion implantation using $B_{10}H_{16}$ or $B_{18}H_{22}$ dopant species. This would increase the 500eV equivalent implant energy to 5keV and 10keV respectively and throughput by as much as 12x up to 180wph (300mm) without any energy contamination in drift mode [2].

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Various plasma doping techniques (PIII and P^2LAD) have been studied over the past 15+ years as an alternative to beam-line implantation and they still remain in development. For P^2LAD the 500eV/1E15/cm^2 equivalent throughput is about 100wph so the cluster ion implantation method would still be 40% higher using traditional beam-line implanters [2]. Only at lower energies (<250eV equivalent) and/or higher doses would plasma doping method have a throughput advantage over beam-line. But all the excess dopant would be electrically inactive therefore of no benefit due to dopant solid solubility limit for USJ applications.

Using in-situ boron doped selective SiGe epitaxy by B_2H_6, box like and super abrupt boron dopant profiles can be realized as reported by Ozturk et al. and shown in Fig.4 [6]. Bohr of Intel reported incorporating this method into their 90nm node [7]. This potentially can result in the elimination of pMOS ion implantation and diffusion-less activation processing and equipment. Also, providing the additional benefits of control localized selective strain-Si technology and elimination of 1 mask level.

3. Dopant Activation/Annealing Roadmap

Used in production since the 130nm node Spike/RTA annealing will be extended to the 65nm node by companies pursuing system-on-a-chip (SOC) LOP and LSTP devices where boron dopant activation limited to 8E19/cm^3 and Xj >20nm is acceptable.

With milli-second annealing times Flash/RTA dopant activation levels of 1.5E20/cm3 can be achieved satisfying the 45nm node HP logic. However, best results are achieved using PAI structures receiving first a 600-700^{o}C intermediate temperature anneal which induces SPE dopant activation followed by the 1250^{o}C Flash anneal as reported separately by Borland et al., Jones and Ootsuka et al. and shown in Fig.5 [1,8,9]. What is limiting the adoption of this technique is the industry wide concerns with Flash annealing equipment maturity and device pattern density optical heating effects.

Laser spike annealing (LSA) is a non-melt surface annealing process with nano-second annealing times. An activation level of 2E20/cm^3 can be achieved satisfying the 32nm node HP logic. Again, industry wide concerns of equipment maturity and use of multiple layer coatings for annealing of device pattern sensitive wafers is limiting its adoption. Another concern with any of these high temperature annealing techniques is its effects on the thermal stability of the gate dielectric material as the industry moves to medium-k (k=12) at the 65nm node and high-k (k=25) at the 45nm node.

Low temperature SPE annealing has achieved dopant electrical activation levels up to 2.5E20/cm3 but process optimization for controlling the location of residual defects and junction leakage is required especially for LSTP logic. For HP and LOP logic devices the leakage levels of SPE formed USJ are acceptable [9,10]. At 600^{o}C SPE regrowth rate is 1nm/second. Ootsuka et al. reported incorporating SPE as part of the sidewall spacer deposition process and no specialized annealing equipment was needed [9]. SPE can also be integrated with other anneals such as Flash/RTA and LSA [9,10].

Fully activated in-situ boron doped selective SiGe epitaxy without additional annealing is being used today at the 90nm node by Intel and boron electrical activation levels up to 1E21/cm^3 can be achieved as reported by Ozturk et al. [6,7]. This far exceeds any implant + activation annealing method including Flash/RTA (1.5E20/cm^3), LSA (2E20/cm^3), SPE (2.5E20/cm^3) and laser melt annealing (5E20/cm^3). Today SEG is only used for pS/D and requires 1 additional mask level but the potential in the future is enormous for single S/D formation, eliminating a mask level and the need for sub-keV implantation and diffusion-less activation annealing equipment. With the additional benefit of controlled localized strain-Si technology without the high costs of blanket SiGe epitaxy with global strain-Si which has a reported cost of $5,000 per 300mm wafer. Several issues with global wafer strain-Si was reported at the 2003 IEDM meeting in comparison to the added benefits of localized strain-Si [11].

4. Junction Measurement/Characterization Roadmap

The 2003 ITRS roadmap defines the USJ requirements as drain extension Xj (nm), maximum drain extension sheet resistance Rs (ohms/square) and lateral abruptness (nm/decade). The industry uses SIMS depth profile to define Xj at a chemical concentration level of 1E18/cm3 for example and abruptness based on the chemical vertical depth profile. Rs is determined from 4PP measurements and the Rs versus Xj chart is created from those values. At 130nm node the USJ target of Xj=35nm and Rs=400ohms/sq. can be achieved with Spike/RTA having approximately 15nm of diffusion and up to 5E19/cm^3 dopant electrical activation level. As the electrical junction depth goes

below 30nm, standard 4PP results become questionable due to probe penetration through the shallow junction. Also, with zero diffusion annealing and dopant activation limited to solid solubility within the PAI region, SIMS can no longer be trusted for determining junction depth, abruptness and electrically activate dopant level.

Due to the 4PP penetrating through the shallow junction, the industry is evaluating non-penetrating 4PP techniques such as Hg-4PP (mercury) or EM-4PP (elastic material). Results from a comparison study between standard 4PP and EM-4PP on junctions ranging from 80nm down to 10nm conducted by Hillard et al. showed the limitation of standard 4PP for junctions below 35nm (Fig.6) [12].

With diffusion-less activation the chemical dopant profile obtained from SIMS is no longer accurate and can be very miss leading so other methods are needed to get the true electrically active dopant profile. Results comparing SIMS to SRP showing the electrically active to inactive chemical dopant profile is shown in Fig.7 [12].

5.Summary

At the 65nm node multiple new methods for USJ pSDE will be used incorporating high tilt PAI and various boron dopant species. Diffusion-less activation will be achieved by the combination of low temperature SPE with high temperature Flash/RTA or LSA. Non-implant doping by in-situ boron doped selective SiGe epi will also be used by some companies. Non-penetrating junction 4PP systems will be used for Rs while electrically active dopant Xj profiles will be characterized by SRP.

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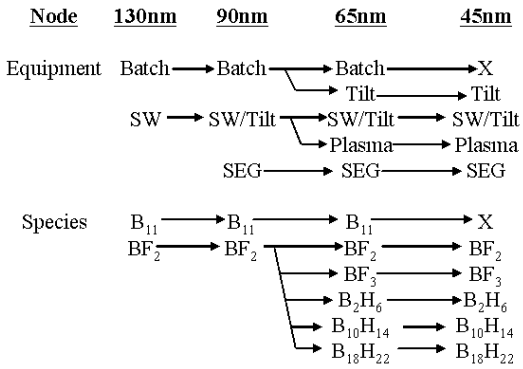

Fig.1: USJ doping roadmap.

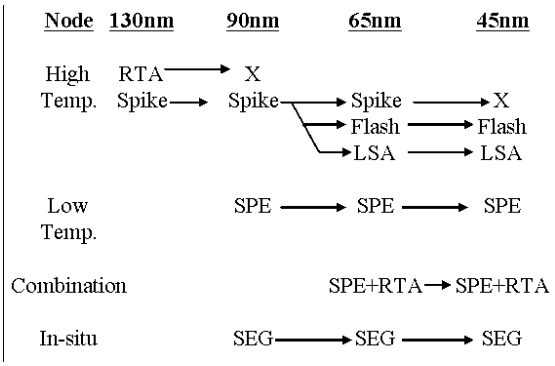

Fig.2: USJ dopant activation & annealing roadmap.

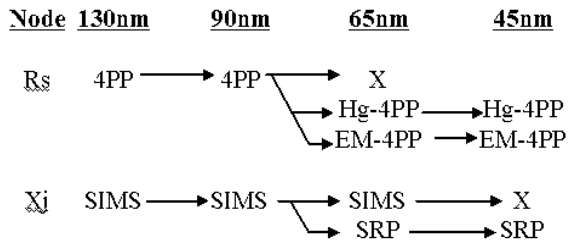

Fig.3: Measurement/characterization roadmap.

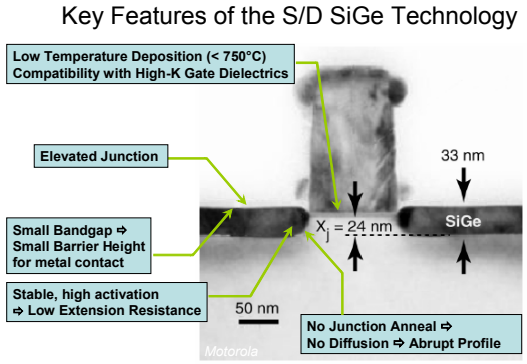

Fig.4: In-situ boron doped selective SiGe epi [6].

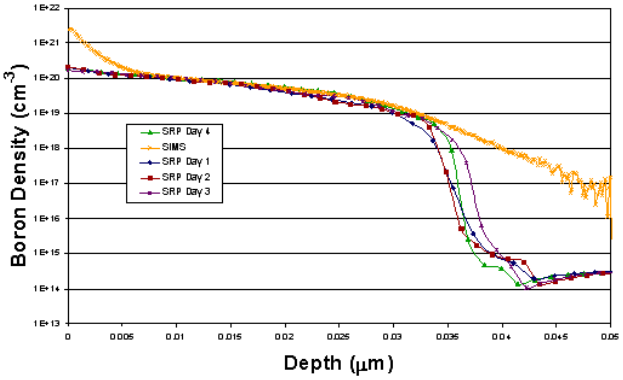

Fig.7: SIMS-vs-SRP comparison [12].

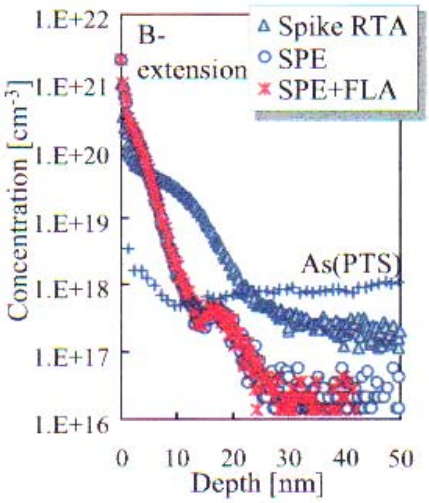

Fig.5: SPE+Flash/RTAfor USJ [9].

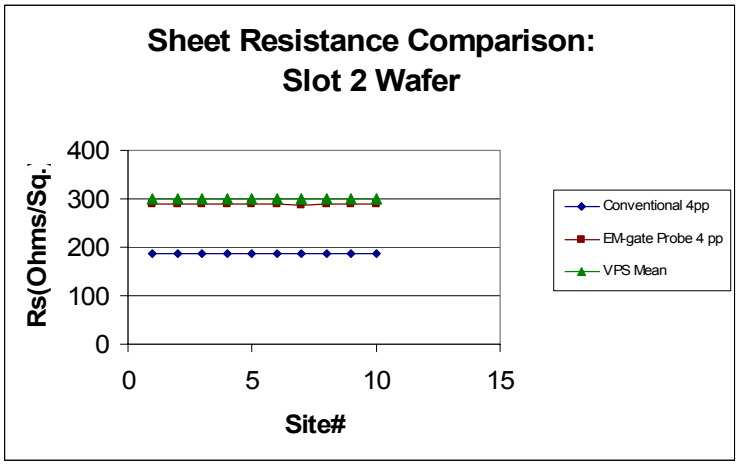

Fig.6: Results from EM-4PP[12].