Alternative USJ Formation & Characterization Methods For 45nm Node Technology

John O. Borland
J.O.B. Technologies
5 Farrington Lane, South Hamilton, MA 01982
Phone: +1-978-808-6271, Fax: +1-978-468-1187, e-mail: JohnOBorland@aol.com

Abstract

Several alternative methods of forming and characterizing ultra-shallow junctions for the 45nm node (Xj=9.5nm) to extend planar single gate CMOS for bulk or SOI technologies are being investigated. To continue gate length scaling (Lg) and optimize gate overlap control, the industry will move from Spike/RTA annealing at the 65nm node to diffusionless activation using high temperature milli-second annealing (Flash/RTA or non-melt laser), low temperature SPE or their combinations to optimize Rs and Xj. This is driving the development of new high dose/low energy implanter designs with: 1) high tilt angle capabilities for gate over lap control, 2) uniform beam parallelism across 300mm wafers to eliminate asymmetrical transistor effects and 3) high productivity at 200eV boron equivalent energies with no energy contamination using new molecular dopant species ($B_{10}H_{14}$ and $B_{18}H_{22}$). If these techniques are unsuccessful in achieving the 45nm node shallow p+ junctions with improved Rs dopant activation above Bss with acceptable junction leakage and device channel mobility enhancement then alternative non-implantation doping methods will be introduced such as in-situ doped SEG and infusion DCD. Also, accurate characterization of these shallow junctions is critical so new non-penetrating 4PP Rs measurement techniques are being developed along with new spreading resistance depth profile analysis to determine the electrically active dopant profile as opposed to the SIMS chemical dopant profile.

Introduction

The ITRS roadmap classifies logic devices as HP (high performance), LOP (low operating power) or LSTP (low stand by power). HP logic devices for desk top PCs will continue to extend SiON gate dielectrics to the 45nm node, requiring the shallowest junctions (9.5nm) with lowest Rs and enhanced channel mobility engineering. Both LOP and LSTP logic devices for portable/mobile applications require long battery life and therefore lowest leakage and will migrate to medium-k (HfSiON, etc.) and high-k (HfO) gate dielectric material with metal gate electrode by the 45nm node as shown in Fig. 1 [1,2]. These low power devices are not aggressively scaled therefore will have deeper junctions (15nm). Medium-k (~15) gate materials such as amorphous HfSiON are thermally stable up to $1050^{o}C$ allowing the continued use of high temperature dopant activation with minimal diffusion if used with polysilicon gate electrode. However, the use of metal gate electrodes will limit thermal processing to $<900^{o}C$. High-k (~25) gate material such as HfO remains amorphous up to $400^{o}C$ if deposited by ALD and $600^{o}C$ if deposited by MOCVD therefore, low temperature SPE dopant activation is the only option.

USJ Doping Methods & Implantation Limits

Challenges facing 9.5nm ultra-shallow junction formation by implantation at the 45nm node for HP logic devices are: 1) >30wph productivity at 300mm, 2) <0.05% energy contamination, 3) no channeling and no residual EOR (end-of-range) damage from PAI causing junction leakage degradation and 4) increased dopant activation above Bss (boron solid solubility) without dopant diffusion. Spike/RTA annealing is being extended to the 65nm node because diffusion-less activation process and equipment such as milli-second flash anneal, laser non-melt annealing or SPE are not yet production ready and the residual EOR damage from the PAI step leads to poor junction leakage after dopant activation, therefore, requiring dopant diffusion beyond the residual EOR damage [3,4]. However, the maximum allowable dopant diffusion for the 45nm node junction depth of 9.5nm is 0-4nm. Also, with these minimal diffusion annealing techniques energy contamination must be kept to <0.05% as reported by Kase to prevent Lg variations as shown in Fig. 2 [5]. With an Lg of 22nm at the 45nm node a 1nm change in lateral gate overlap results in a 2nm (10%) change in Lg. Table 1 shows comparison of boron implant energy to achieve the desired 9.5nm deep USJ at $1E18/cm^3$ for a $1E15boron/cm^2$ implant for various monomer and molecular dopant species with and without PAI to reduce channeling effects. With B_{11} and no diffusion an energy of <100eV would be required and with 4nm of diffusion <50eV. Using PAI would increase the energy to 250eV and 125eV respectively. Decaborane and octa-decaborane would increase the energy by 10x and 20x respectively making it feasible using current beam-line implanters and their effective boron beam current is shown in Fig. 3 [6]. Hamamoto et al., also observed self-amorphization by X-TEM using $B_{10}H_{14}$ compared to B_{11} at 500eV and a dose of $1E15/cm^2$ [7].

<u>USJ Dopant Activation Issues:</u> Due to Bss limit in silicon both Spike/RTA and Flash/RTA dopant activation annealing can only

achieve 3-6E19/cm^3 dopant electrical activation for beam-line and plasma doping techniques. Using Ge-PAI to eliminate channeling Ito et al. also reported improving B activation by 4x with flash annealing from 2660ohms/sq. (3E19/cm^3) to 770ohms/sq. (1.2E20/cm^3) as shown in Fig. 4 [8]. However, one issue with diffusion-less activation is residual EOR damage from PAI leading to junction leakage degradation [3,4]. With diffusion-less activation to achieve the desired lateral dopant placement for SDE gate overlap control high tilt (up to 30 degrees) low energy implantation is necessary as reported by Borland et al. [9]. Fig. 5 shows the relationship between nSDE implant tilt angle on gate overlap and nMOS device drive current [10]. A 30 degree tilt angle results in 0.5x lateral to vertical junction depth profile. This is one of the reasons for the introduction of new single wafer high current implanters and medium current multi purpose implanter (MPI) [6]. Batch high current implanter with a tilt capability of 45 degrees is also able to do these high tilt SDE implants as reported by Wan et al. [11]. Another issue with reduced diffusion is asymmetrical transistors caused by cone angle effects with batch high current implanters as reported by Yoneda & Niwayama [12]. This 1.2 degree tilt angle variation across a 300mm wafer can be corrected as reported by Wan et al. using a "cone angle corrective pad" on their batch high tilt high current implanter [11].

USJ Metrology Issues: As junctions scale below 30nm, 4 point probe penetrating through the junction leads to incorrect Rs measurements as shown in Fig. 6 [13]. This has lead to the development of non-penetrating 4PPs such as EM-4PP (elastic material) to measure Rs more accurately. As the industry moves to diffusion-less activation at the 45nm node other techniques besides SIMS are required to determine the electrical junction depth because the difference between the electrically active dopant level and chemical dopant level in the USJ structure can be over an order of magnitude, therefore, new alternative implanter dose monitoring techniques such as XPS are under evaluation.

Improving Dopant Electrical Activation: A SiGe alloy mixture increases Bss and in a 20% SiGe material Lee et al. reported a 2x increase in boron sheet carrier concentration [14]. Ozturk reported a 5x improvement in Bss (1E21/cm^3 versus 2E20/cm^3) using a 500°C SiGeB in-situ doped SEG (selective epitaxial growth) process [15]. Using GCIB (gas cluster ion beam) no channeling is observed with this infusion doping technique and box-like dopant profile engineering can also be achieved [16]. Self-amorphization without residual EOR damage is also realized and using B+Ge infusion doping, improved Bss by 2x was observed by SIMS analysis resulting in lower Rs value [16].

Channel Mobility Engineering

Enhanced device channel mobility is critical for continued device scaling due to channel mobility degradation caused by both gate dielectric scaling and increased channel doping level as reported by Ghani et al. and Samavedam et al. [1, 17]. Due to the high wafer costs ($>4K/300mm wafer) and defects levels (>2E5/cm^2) blanket epitaxial strain-si on relaxed SiGe on silicon wafers will not be adopted by the industry, instead localized strain allowing for the optimization of strain for nMOS and pMOS independently has been adopted by the industry starting at the 90nm node. Ghani et al. reported on using SiGeB SEG for pS/D to induce compressive strain for p-channel devices and improve Bss [18]. Chidambaram et al. also reported using SiGeB SEG for the pSDE to further improve pMOS device performance by 35% [19]. This can also be achieved with Ge+B infusion doping into the pSDE as shown in Fig.7 at room temperature using photoresist patterning without the need for a hard mask and complicated processing steps of; 1) silicon amorphization, 2) silicon etching, 3) surface cleaning, 4) high temperature SiGeB SEG selectivity and facet control deposition and 5) hard mask removal [16]. To improve channel mobility by >2.5x the industry is now starting to investigate devices with Ge channel. By increasing the Ge infusion dose to >1E15/cm^2 dose controlled deposition (DCD) can be realized and Fig.8 shows results for SiGe infusion DCD at various controlled Ge percentages from 20-75%.

Summary

At the 45nm node HP logic device requirements will require molecular dopant species such as $B_{10}H_{14}$ and $B_{18}H_{22}$ and diffusionless activation to realize the 9.5nm USJ target. However, due to the enhancement in channel mobility and Bss to improve pMOS device performance alternative doping methods such as SiGeB SEG and Ge+B infusion doping are potential replacements to low energy implantation. For LOP & LSTP logic devices the USJ target is relaxed to 15.0nm so traditional implantation can be used with high tilt batch or single wafer low energy implanters for SDE gate overlap control with diffusion activation techniques. High temperature diffusionless activation maybe introduced with poly gate electrode but low temperature activation will be required with metal gate electrodes and high-k gate dielectrics. Non-penetrating EM-4PP for Rs measurements and x-ray analysis for implant dose monitoring will also be adopted for USJ process and implanter dose monitoring.

References

[1] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi and M. Bohr, VLSI Sym. June 2000, section 18.1, p. 174.
[2] J. Borland, Solid State Technoloy gate stack webcast, July 1, 2004.

[3] R. Lindsey et al., *Advanced Short-Time Thermal Processing for Si-Based CMOS Devices II*, the Electrochemical Society, PV 2004-01, p.145.

[4] J. Borland, T. Matsuda and K. Sakamoto, Solid State Technology, June 2002, p.83.

[5] M. Kase, vTech 2004 presentation material, July 2004.

[6] J. Borland, M. Tanjyo, N. Nagai, T. Aoyama and D. Jacobson, Semiconductor International, Jan. 2005, p.52.

[7] N. Hamamoto, S. Umisedo, T. Nagayama, M. Tanjyo, S. Sakai, N. Nagai, T. Aoyama and Y. Nara, 15th International Conference on Ion Implantation Technology, Oct. 2004, paper F251 to be published.

[8] T. Ito et al., IWJT 2002, p.23.

[9] J. Borland, V. Moroz, H. Wang, W. Maszara and H. Iwai, Solid State Technology, June 2003, p. 52.

[10] J. Borland, vTech 2003 presentation material, July 2003.

[11] Z. Wan, T. Lin and J. Chen, 15th International Conference on Ion Implantation Technology, Oct. 2004, paper A362 to be published.

[12] Yoneda and Niwayama, IWJT 2002, p. 19.

[13] R. Hillard, R. Mazur, C. Ye, M. Benjamin and J. Borland, Solid State Technology, Aug. 2004, p. 47.

[14] K. Lee et al., IEDM-2002, section 14.7, p. 379.

[15] M. Ozturk, N. Pesovic, J. Liu, H. Mo, I. Kang and S. Gannavaram, *Semiconductor Silicon 2002*, the Electrochemical Society, PV 2002-2, p.761.

[16] J. Borland, J. Hautala, M. Tabat, M. Gwinn, T. Tetreault and W. Skinner, *SiGe: Materials, Processing And Devices*, the Electrochemical Society, PV 2004-07, p. 769.

[17] S. Samavedam et al., IEDM-2002, sect. 17.2, p. 433.

[18] T. Ghani et al., IEDM-2003, section 11.6, p. 978.

[19] P. Chidambaram et al., VLSI Sym. 2004, section 6.1, p.48.

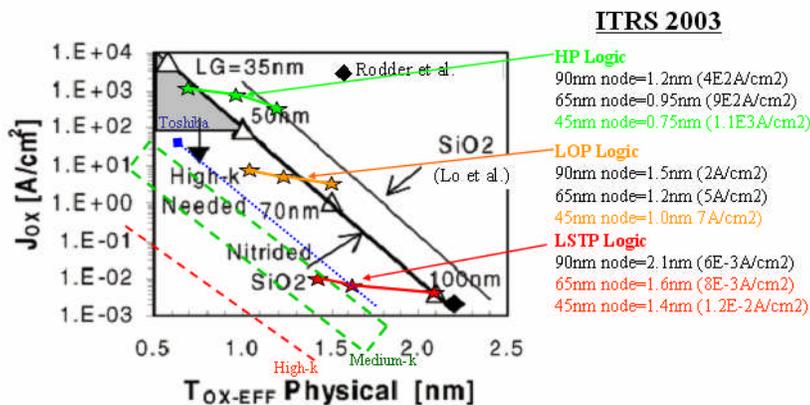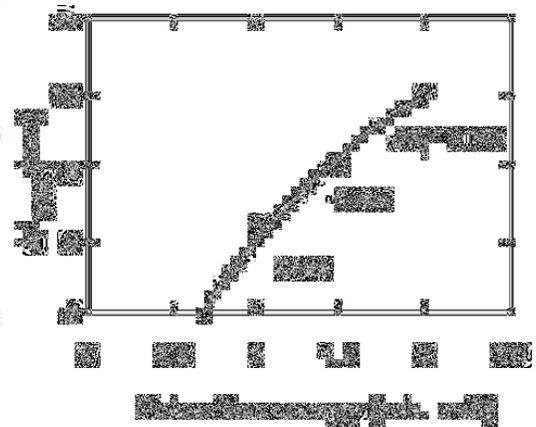Fig. 1: Gate dielectric ITRS roadmap [2].

Fig. 2: Influence of decel energy contamination on Lg variation [5].

Table 1: Drift-Mode Boron Implant Energies

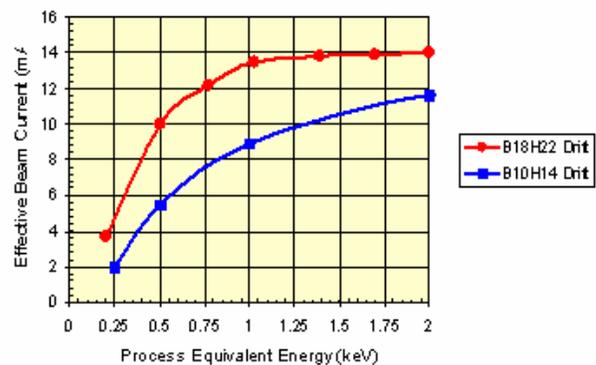|	LOP & LSTP 45nm Node Xj=15nm	HP 45nm Node Xj=9.5nm	HP If 4nm diffusion
B_{11}	200eV	<100eV	<50eV
PAI+B_{11}	500eV	250eV	<125eV
BF_2	880eV	200eV	<100eV
PAI+BF_2	2.2keV	1.5keV	<750eV
$B_{10}H_{14}$	2keV	1keV	<500eV
PAI+$B_{10}H_{14}$	5keV	2.5keV	<1.2keV
$B_{18}H_{22}$	4keV	2keV	<1keV
PAI+$B_{18}H_{22}$	10keV	5keV	<2.5keV

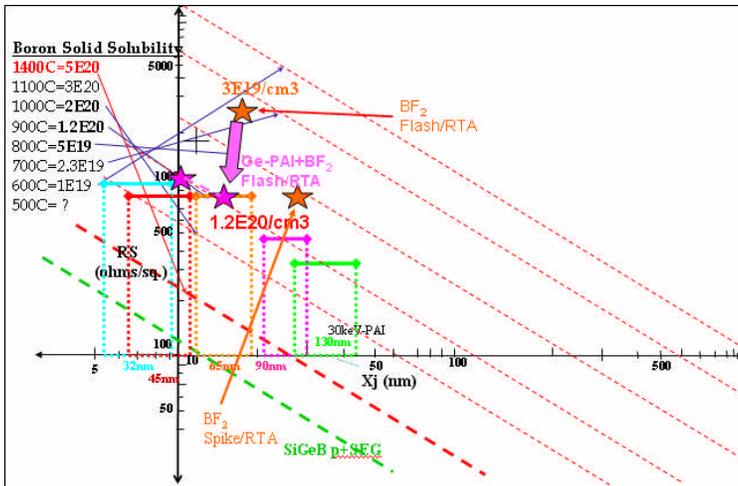Fig. 3: Effective beam current ($B_{10}H_{14}$ & $B_{18}H_{22}$) [6].

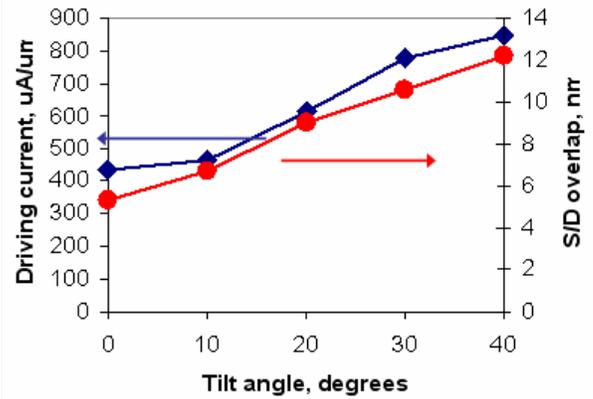Fig. 4: Rs versus Xj comparison, Ge-PAI improves Rs by 4x.
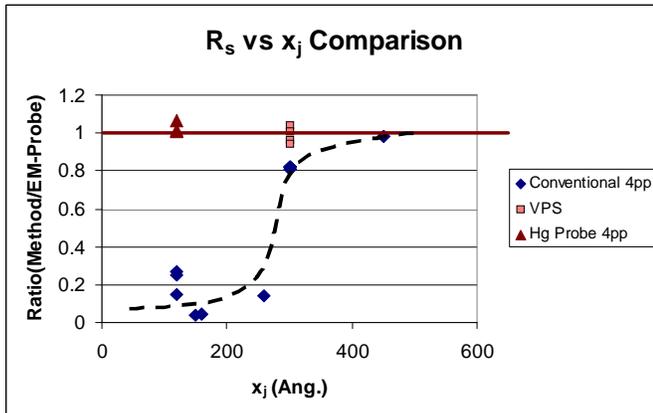

Fig. 5: Tilt angle effects [9].

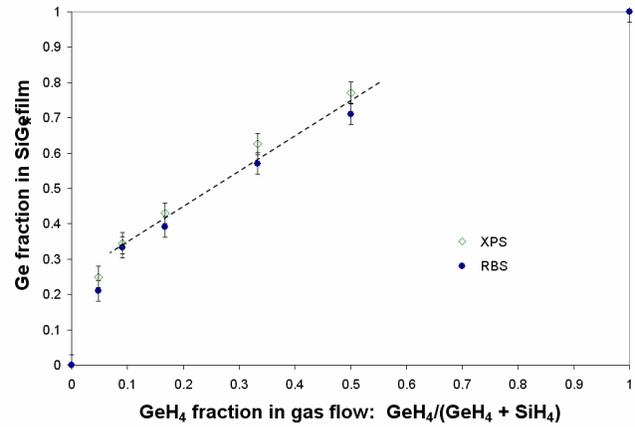Fig. 6: 4PP penetration as Xj scales below 30nm [12].
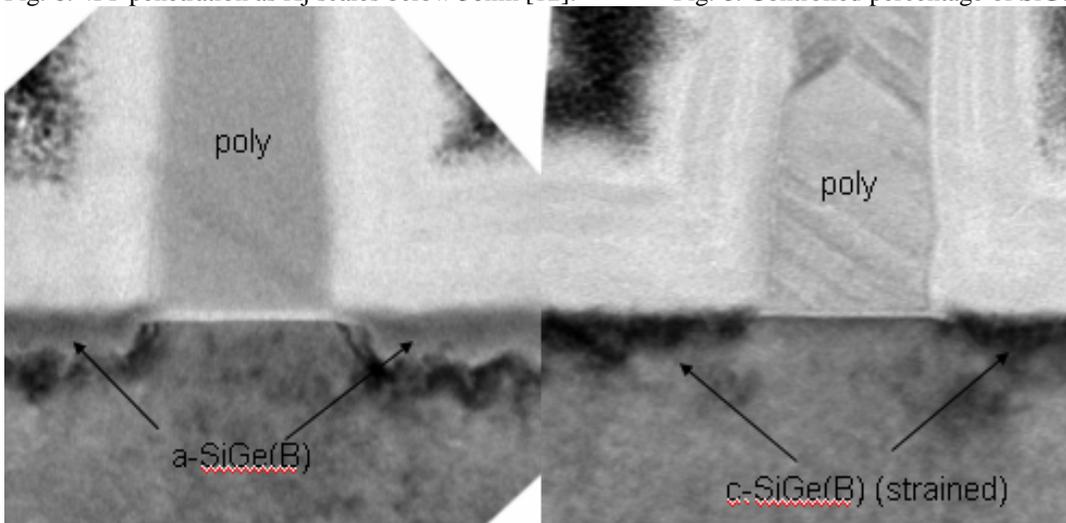

Fig. 8: Controlled percentage of SiGe infusion DCD.

Fig. 7: Ge+B infusion doping for pSDE localized strain-Si [15].