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FEOL
FRONT END OF LINE

Extending the life of planar CMOS with multigate CMOS devices

As the industry continues to scale devices to meet the various system-on-a-chip (SoC) applications in the future, several types of transistor designs from planar to vertical single-gate (SG), double-gate (DG), and multigate (MG) are emerging as are several options in silicon starting material (bulk CZ, Epi, blanket SOI, and selective/patterned SOI wafers) [1]. Although planar SG device scaling has been demonstrated down to a gate length (L_g) of 6nm, the end of the roadmap for planar SG CMOS seems to be drawing nearer as the industry increases research activities in DG and MG CMOS devices. Multiple device roadmaps that depend on specific applications are also emerging [2]. Both logic and memory devices will migrate from planar structures to vertical structures; Fig. 1 shows various DG to MG design options [3, 4].

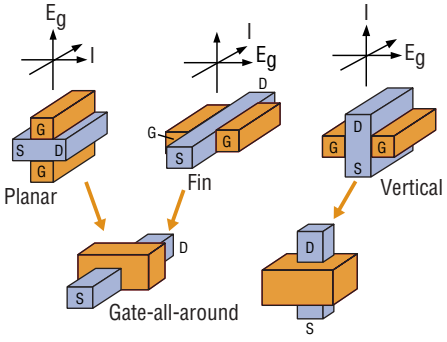

Figure 1. Double-gate to multigate CMOS structures [3]. E_g = gate field direction; I = channel current direction.

Single-gate structure

There is no fundamental change in the design of the planar SG transistor through the end of the roadmap. However, changes for improved device performance will be made for its scaling and extendibility. The current oxynitride gate dielectric material will first evolve to a medium-*k* of 12 at the 65nm node and then to a high-*k* of 25 at the 45nm node. The possible design evolutions of the transistor channel and source drain (S/D) region are shown in Fig. 2. Starting at the 90nm node, higher-dose HALOs (super HALO) for short channel effect (SCE) control will be used, which will degrade channel mobility due to impurity scattering, leading to the adoption of a strain-Si channel. This strained Si technology can be avoided, however, with the lateral graded source drain extension (LG-SDE) structure (Fig. 3), which improves lateral abruptness, gate overlap control, and R_{ext}, thereby reducing the HALO dose [2, 5].

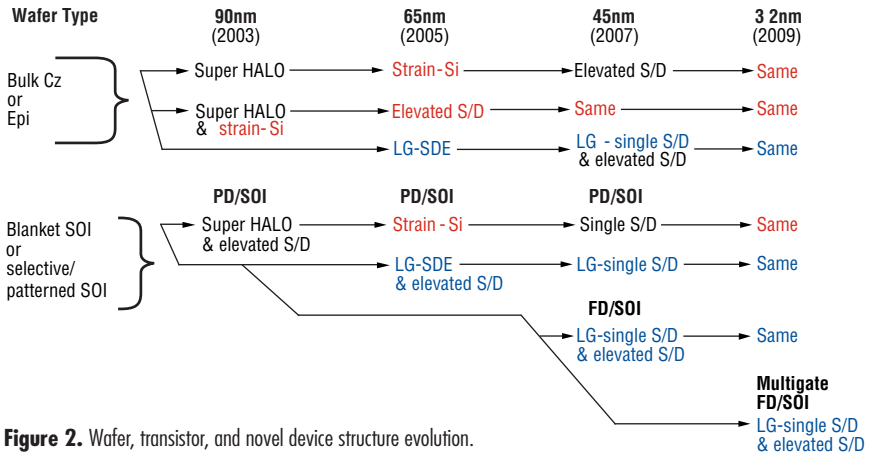

Figure 2. Wafer, transistor, and novel device structure evolution.

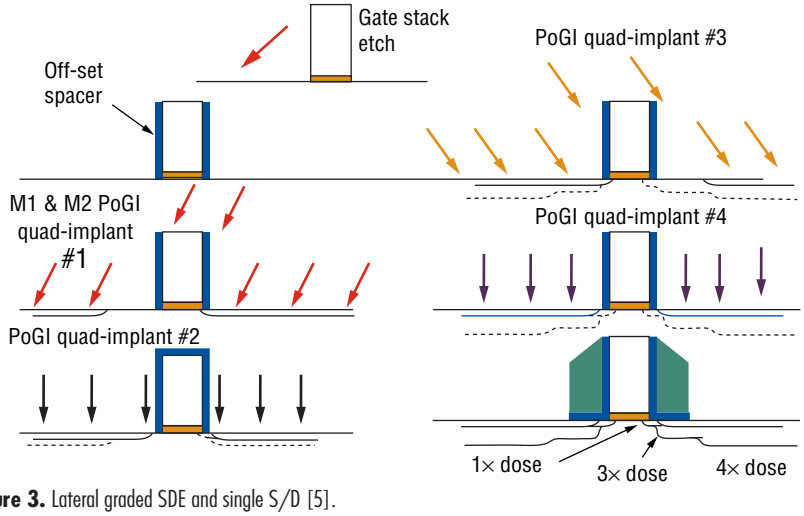

Figure 3. Lateral graded SDE and single S/D [5].

Undoped elevated S/D structures for improved salicide contacting will first be used for thin (<50nm thick) partially depleted SOI (PD/SOI) devices at the 90nm node to maintain good salicide S/D contacting [6]. Because the PD/SOI layer is so thin, however, the depth of the SDE will be the same as the SOI thickness, so merged SDE and deep S/D junctions into single-S/D and LG-SS/D structures for lower S/D

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tip resistance for thin PD/SOI devices will begin at the sub-65nm node. The switch from $CoSi_2$ to $NiSi_2$ salicide for lower S/D contact resistance and poly gate resistance will start at the 90nm node for lower contact and gate/poly resistance, lower temperature processing, and compatibility with SiGe material used in strained Si technology.

Double/multigate CMOS

With difficulties expected in future scaling of SG fully depleted SOI (FD/SOI) devices, the industry is rapidly looking at DG and MG FD/SOI devices starting at the sub-45nm node for L_g<20nm. This would ease SOI wafer manufacturing, since the SOI thickness will be 0.7–1× L_g compared to SG FD/SOI, where SOI thickness is 0.2–0.3× L_g!

Other benefits include better SCE control and higher drive current [3].

Another significant FEOL process change starting at the 65nm node will be the integration of diffusion-less activation (high-temperature or low-temperature annealing) to achieve the shallow SDE junction requirements [7]. With either diffusion-less activation method, disposable spacer (reverse S/D) process flow will be needed, allowing high-temperature diffusion for gate/poly doping and deep S/D junction formation. For the 45nm node and beyond, higher SDE activation levels will require low-temperature SPE exclusively. To achieve the desired SDE gate overlap control with diffusion-less activation, high-tilt, post-gate implant (PoGI) SDE implantation will be used starting at the 65nm node. ■

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