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Equipment Basics

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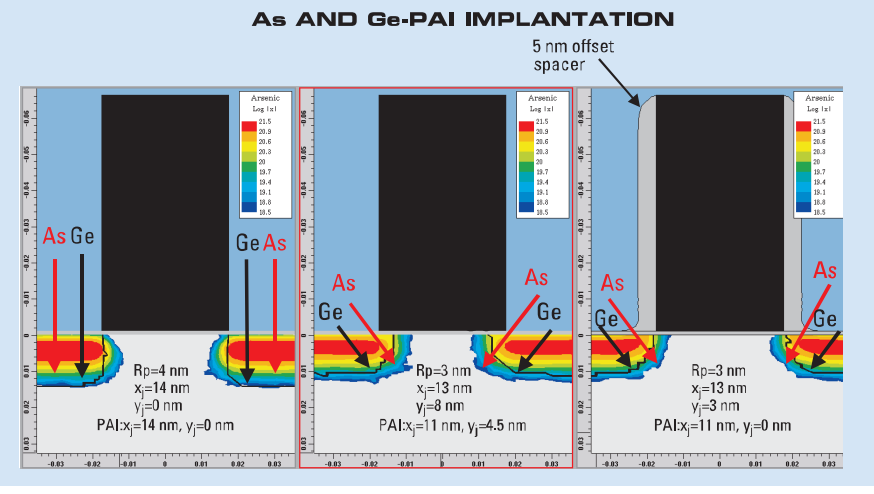
Implantation and Annealing Options for 65 nm Node SDE Formation

Starting at the 65 nm node with a gate length (L_g) of 35 nm, the industry is forced to move to diffusionless activation for the critical ultrashallow junction (USJ) requirements of x_j=15 nm and gate overlap control of y_j>8 nm for the source/drain extension (SDE) structure, especially for PMOS transistors to suppress boron diffusion. The two choices for diffusionless activation are either high-temperature or low-temperature activation/annealing.[1,2] The three approaches being pursued for high-temperature activation are: 1) spike/RTA annealing with rapid cool-down/quenching for <10 nm of diffusion[3]; 2) flash/RTA annealing using a two-step process of low-temperature heating of 400-800°C followed by flash lamp heating of 1100-1350°C for <10 msec to achieve <4.0 nm of diffusion[4]; and 3) sub-melt laser annealing to realize <1 nm of diffusion.

Low-temperature activation using pre-amorphizing implantation (PAI) with germanium or silicon followed by solid-phase epitaxial (SPE) regrowth in the 500-650°C temperature range for a few minutes has produced USJs satisfying the 23 nm node targets of x_j=6 nm and R_s=1015 Ω/sq.[5] The current 90 nm node 1.2 nm equivalent oxide thickness (EOT) oxynitride gate dielectric material will first evolve to 0.8 nm EOT medium k of 12 (HfSiON, HfO_2/Al_2O_3, etc.) at the 65 nm node, and then to 0.6 nm EOT high k of 25 (HfO) by the 45 nm node. High-temperature diffusionless activation can be used with medium-k gate dielectrics, but once true high-k gate dielectrics are implemented, only low-temperature diffusionless activation can be used to maintain their amorphous phase and high-k integrity.

Diffusionless high-tilt implantation for SDE

Ghani et al.[6] reported that SDE vertical junction depth (x_j), lateral junction depth (y_j) gate overlap/under diffusion, and lateral abruptness can be optimized to maximize device drive current. The ratio of the roadmap targeted SDE lateral gate overlap (y_j) to vertical junction depth (x_j) is ~0.5.[2] Using a new Taurus Monte Carlo implant model just developed by Synopsys, diffusionless activation simulation results for 65 nm node devices (L_g=35 nm, height=65 nm and t_{ox}=0.8 nm) is shown in the Figure for NMOS arsenic 3 keV/1 ˘ 10^{15}/cm² implant with Ge-PAI 10 keV/5˘10^{14}/cm² with 0 and 30° tilt. For NMOS transistors, the y_j gate overlap target of >8 nm could not be achieved for 0° tilt (0 nm overlap), shown at left; while the 30° high-tilt case y_j=8 nm resulted in a y_j/x_j=0.61 (center). With the 5.0 nm sidewall offset spacer, y_j was reduced to 3.0 nm (right). Geometrically, sin10°=0.17, sin20°=0.34 and sin30°=0.5, so a 30° tilted implant is ideal for the targeted gate overlap ratio of 0.5.



Taurus Monte Carlo implant simulation comparison of 0° tilt (left) vs. 30° quad-mode implant for As 3 keV/1 ˘ 10^{15} and Ge-PAI for gate overlap control and optimization of lateral dopant profile when using diffusionless activation (center). With the 5 nm sidewall offset spacer, y_j was reduced to 3 nm (right).

Since the as-implanted profile is the same as the final profile with diffusionless activation, ion implantation and dopant activation can now be decoupled. Also, high-tilt (30°) quad-mode directional implantation in the lateral di-

mension is desirable to precisely control gate overlap (encroachment) for the 65 nm node and beyond. Therefore, high-tilt SDE formation is now on the roadmap of several companies starting at the 65 nm node. Most high-temperature and all low-temperature diffusionless activation processes are using some form of PAI to achieve maximum dopant activation. For the precise control of gate overlap and optimization of lateral dopant activation, the PAI step will also require high tilt. Simulation comparison of 10 keV Ge-PAI at 0 vs. 30° tilt is also shown in the Figure to create the lateral graded SDE (LG-SDE) structure.[7] Outlined in black is the simulated amorphous/crystalline silicon interface vertically under the junction and laterally under the gate. No lateral placement under the gate sidewall for 0° tilt was observed, while 4.5 nm (y_j/x_j=0.41) lateral placement under the gate with the 30° tilt was achieved. Using the 5 nm offset spacer in the Figure (right) positions the PAI amorphous/crystalline interface at -0.5 nm y_j gate overlap. Therefore, high-tilt dopant and PAI implantation will allow precise optimization and engineering of lateral dopant activation for gate overlap control when using diffusionless activation (high- or low-temperature) processing. The potential device performance benefits of the LG-SDE structure are: 1) improved gate overlap control and short channel effect due to shallower junction (x_j), more gate overlap (y_j) and good lateral abruptness; 2) reduction in HALO dose so there is no channel mobility degradation, thereby delaying the need for strained silicon channel technology; 3) reduced gate overlap capacitance and junction capacitance; and 4) improved I_{dsat} and increased ring oscillator speed due to lower R_{ext}.[7] •

References

1. J. Borland, T. Matsuda and S. Sakamoto, "Shallow and Abrupt Junction Formation: Paradigm Shift at 65-70nm," *Solid State Technology*, June 2002, p. 83.

2. J. Borland, "Low Temperature Activation of Ion Implanted Dopants: A Review," extended abstract, the *International Workshop on Junction Technology*, December 2002, p. 85.

3. T. Matsuda, "Shallow Junction Technologies to Meet the 65nm Node: High Temperature vs. Low Temperature Activation," vTech/Japan 2002 seminar presentation material, December 2002.

4. T. Ito, et al., "Flash Lamp Annealing Technology for Ultra-shallow Junction Formation," extended abstract, the *International Workshop on Junction Technology*, December 2002, p. 23.

5. S. Felch, et al., "Optimized BF_3 P^2LAD Implantation With Si-PAI for Shallow, Abrupt and High Quality p^+/n Junctions Formed Using Low Temperature SPE Annealing," IIT-2002, September 2002, Taos, N.M., to be published.

6. T. Ghani, et al., "Scaling Challenges and Device Design Requirements for High Performance sub-50nm Gate Length Planar CMOS Transistors," *IEEE 2000 VLSI Sym. Proc.*, Section 18.1, June 2000, p. 174.

7. J. Borland, H. Iwai, W. Mazara and H. Wang, "Extending Planar Single-Gate CMOS & Accelerating the Realization of Double-Gate/Multi-Gate CMOS Devices," ECS Spring Meeting, ULSI Process Integration III, April 2003, to be published.