EXTENDING PLANAR SINGLE-GATE CMOS & ACCELERATING THE REALIZATION OF DOUBLE-GATE/MULTI-GATE CMOS DEVICES

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ABSTRACT

The end of the roadmap for planar single-gate (SG) CMOS seems to be drawing nearer as the industry increases research activities in double-gate (DG) and multi-gate (MG) CMOS novel device structures. Therefore, this paper will focus on how to extend the life of planar SG CMOS through 2016 and accelerate the understanding & realization of MG CMOS by 2007 through the use of advanced ion implantation techniques. The most critical area in future transistor design for improved device performance will be lateral and vertical source drain (S/D) engineering for SG, DG & MG transistor formation with CMOS bulk, epi or SOI technologies and the realization of new novel device structures to satisfy the current and future ITRS device application roadmaps.

INTRODUCTION

The 2001 ITRS roadmap classifies logic devices into three different categories: 1) high performance (HP) logic devices for desktop computers which are highly scaled, highest performance and highest leakage current requiring very thin oxy-nitride gate dielectrics, low S/D parasitic resistance and enhanced channel mobility, 2) low operating power (LOP) logic devices for portable mobile systems with limited battery life like for notebook computers requiring high performance but lower leakage current and 3) low standby power (LSTP) logic devices for cell phones having low performance and lowest leakage current (1). Low leakage to extend battery life is most critical for low power logic devices therefore gate leakage reduction through migration to medium-k first (k=12) and then high-k (k=25) gate dielectrics and reducing junction leakage through thin SOI will be required in the next few years. Therefore, multiple device roadmaps are emerging depending on their application as shown in Fig.1 (2). Different logic and memory applications will also require variations in transistor design from HALO to Super HALO, strain-Si channel for mobility improvement, S/D extensions (SDE) with elevated S/D to lateral graded SDE (LG-SDE) and single S/D (LG-SS/D). Novel device structures will also vary from planar SG to vertical SG and eventually to DG and MG devices (Fig.2&3) (3,4). With the integration of these various transistor designs and novel device structures on the same chip for system-on-chip (SOC), new silicon wafer options are also emerging from traditional bulk Cz and Epi wafers to blanket SOI and new selective/patterned SOI wafers for partially depleted (PD)/SOI and fully depleted (FD)/SOI devices as shown in Fig.4 for 90nm, 65nm and 45nm technology nodes (5-8).

MOS-FET Transistor Design Evolution From SG To DG & MG

SG planar CMOS transistor scaling has been demonstrated down to gate length (Lg) of 6nm for logic devices as reported by Ieong et al (9). For DRAM trench capacitor cell designs, vertical SG transistors will be needed to continue scaling as reported by Divakaruni et al. and shown earlier in Fig. 2 (3). DG transistors have also been demonstrated at various Lg from 200nm down to 10nm in both the planar and vertical configurations as illustrated in Fig. 3 (4,7,10-16). Therefore, the question becomes when if ever will be the end of the roadmap for planar SG CMOS devices and can we realistically extend SG manufacturing to Lg=6nm over the next 15 years or will manufacturing costs and device performance limitations drive the move to DG & MG CMOS devices sooner.

SINGLE-GATE CMOS

There is no foreseeable change in the fundamental design of the planar SG transistor through the end of the roadmap whether bulk, epi, or SOI technologies are used. However, changes for improved device performance will be made in the gate stack structure with the move to higher-k gate dielectric material and metal electrode. Also, several changes are possible in the transistor channel, source drain and contact region through dopant and material engineering such as: 1) higher dose super HALO (17), 2) LG-SDE for gate overlap control, improved lateral abruptness and short channel effect (SCE) control (7), 3) merged single S/D structures for lower resistance (18,19), 4) elevated S/D structures for improved resistance and silicide contacting (7), 5) new silicide material such as $NiSi_2$ for lower contact resistance and gate poly resistance (2) and 6) strain-Si technology for channel mobility improvement (20,21). Most companies will continue to use deep S/Ds with bulk and epi wafers for good silicide contacting, low junction leakage and low S/D parasitic resistance while elevated S/Ds will first be used with PD/SOI devices at the 90nm node as film thicknesses go below 50nm limiting the amount of silicon available for silicide consumption and to achieve good contact formation. Also, super HALO at higher doses will be critical to control SCE and Vt thus eliminating the traditional Vt channel doping implant starting at the 90nm node. The move to epitaxial strain-Si layer for channel mobility enhancement has been on the SOI and high-k dielectric roadmaps for several years now but due to the high defect levels ($10^5/cm^2$) compromises in the amount of strain-Si have been made so other methods to induce localized strain-Si have also been developed without the use of epitaxy.

300mm Silicon Wafers Options:

For improved silicon material quality at 300mm, a majority of IC manufacturers have switched to Epi wafers to maximize yield. Growing an epitaxial silicon layer on top of bulk Cz wafers eliminates grown in defects such as COP (22). For this same reason, SOI wafers are also using a top epitaxially grown silicon layer for both the SIMOX and wafer bonding manufacturing methods in order to achieve highest SOI silicon layer quality (23). The transition to 300mm has now been under way for 5 years starting back in 1997 at Infineon and will continue for the next 8 years before the expected first introduction of 450mm wafers in 2010.

Blanket SOI Wafers. In order to further reduce SIMOX manufacturing costs, the MLD (modified low dose) process was developed by researchers at IBM (5). Today there are 2 suppliers of 300mm oxygen implanters for SIMOX technology, IBIS in the US and

Hitachi in Japan. SOITEC in France, ELTRAN in Japan and Silicon Genisis in the US manufacture thin bonded SOI wafers. SOITEC uses hydrogen implantation induced wafer cleaving, Silicon Genisis uses combined hydrogen implantation with SiGe strain layer epitaxy for nano cleaving and ELTRAN uses epitaxy over porous silicon to induce cleaving (23). One of the main challenges for thin SOI wafer manufacturing is scaling the film thickness with each technology node while maintaining tight uniformities. At 180nm node the SOI film thickness for PD/SOI devices was 160-170nm. For 130nm node the SOI film thickness was reduced to a range between 79-120nm and for the 90nm node the film thickness range is expected to be between 30-60nm therefore, PD-SOI film thickness is approximately equal to Lg (5,17). With thinner SOI films, tighter control on thickness uniformity is critical since this directly defines the device channel region and variations will directly impact Vt control as shown in Fig. 5 and ring oscillator delay as reported by Shahidi (17). For FD/SOI devices the SOI film thickness is targeted to be about 0.2-0.3x Lg so at 90nm node with Lg=50nm the FD/SOI film thickness will be 10-15nm and at 65nm node with Lg=30nm the SOI film is expected to be only 6-9nm thick (4). Very thin SOI film thickness uniformity and control for these fully depleted devices will be a major challenge especially for bonded SOI wafer manufacturers in the future. Again, as mentioned above, as the SOI top silicon film gets thinner S/D parasitic resistance goes up and contacting silicide becomes a problem requiring the use of elevated S/D structures.

Patterned/Selective SOI Wafers. For embedded memory and other SOC applications, logic devices on SOI material and memory devices on bulk material may be preferred. Therefore, two different approaches to realize logic devices in SOI and DRAM trench capacitor memory devices in bulk (non-SOI) have been recently reported. Researchers at IBM reported using the SIMOX method with a patterned mask for the oxygen implant resulting in regions on a bulk wafer with patterned SOI structures as shown in Fig.6a (5). Other researchers at Toshiba reported using the bonded SOI wafer approach with patterned etch back through selected SOI regions down to the bulk wafer followed by selective epitaxial growth in these non-SOI regions forming selective SOI shown in Fig.6b (6). Other SOC embedded device applications include bipolar RF devices where the vertical SiGe bipolar device can be on bulk (non-SOI) or SOI material (17).

Lateral Device Isolation Improvements

Shallow trench isolation (STI) is still the standard isolation structure however, well to well and n+ to p+ device isolation is becoming limited by tilted high energy implantation mask shadowing and encroachment (23-26). For high packing density SRAMs, improved n+ to p+ device isolation with 15% cell size reduction was reported by Yamashita et al. for sub-90nm embedded SRAM when they went to zero degree tilt for the high energy well implants (24). At 90nm and below requiring <0.3um n+ to p+ spacing, zero tilt high energy implantation with precise implant angle control and beam parallelism will be necessary to maintain uniform across wafer device parametrics with tightest packing density (25, 26).

Gate Stack Evolution

The gate dielectric material has evolved from silicon dioxide (SiO_2) to oxynitrides (SiON) and nitride/oxide (SiN/SiO_2) sandwich structures as the gate thickness scaled below 2.2nm to the current range of 1.2nm at 90nm node. To reduce gate leakage for low

power CMOS higher dielectric constant materials are needed so medium-k (k=12) gate dielectrics like HfSiON and HfO_2/Al_2O_3 may be used first before going to true high-k (k=25) dielectrics like HfO [2,27-29]. There are still major manufacturing and integrations issues before medium-k and high-k gate dielectrics can be used such as surface interface control and surface mobility degradation along with fundamental mature deposition equipment and a stable process. The gate electrode will also evolve from current poly-Si to poly SiGe and then to metal. Again, much R&D still needs to be done before a replacement gate electrode to polysilicon can be implemented.

Channel Evolution

As Lg scales, HALO dose increases (super HALO) to improve SCE (short channel effects) and reduce Vt roll-off but if the dose is too high reverse short channel effect (RSCE) occurs as illustrated in Fig. 7 for super HALO with PD/SOI (17). Also, as Lg shrinks, at some point the HALOs will begin to overlap as shown in Fig.8 thereby increasing the transistor channel region doping level into the upper E18 to lower E19/cm^3 level thereby degrading channel mobility (2,16,30). For sub-50nm Lg, Vt implants may be dropped and HALO implants will be used to control Vt for bulk and SOI devices. As the channel concentration increases above 2E18/cm^3 for Lg <50nm for SCE control, mobility degrades as reported by Ghani et al. and shown in Fig.9 (30). This leaves only three options: 1) either improve channel mobility through the implementation of strain-Si channel technology as announced recently by Intel for 90nm node SRAM (21), 2) reduce HALO dose (channel doping concentration) through SD engineering with improved SDE lateral abruptness and ultra shallow junction as realized through LG-SDE for Lg<50nm (7,31) or 3) move to FD-SOI having SG or DG transistors with light to no doping in the channel (11,12,16). Options 2 and 3 will be described latter. Improved electron mobility for strained-Si on either SiGe bulk or SiGe/SOI wafers was reported by Z. Cheng et al. (20). A thin strained silicon epilayer on top of relaxed SiGe buffer epilayer has been reported to increase mobility by up to 1.8x for electron mobility and less for hole mobility. This technique can also be applied to SOI wafer manufacturing called SSOI (strained silicon on insulator) or SGOI (SiGe SOI) as reported by IBM using wafer bonding SOI and Toshiba with SIMOX SOI though much more defect reduction is still needed to realize a thin PD/SSOI or PD/SGOI strain-Si layer structure especially for SIMOX wafer technology (5,32). The best strain-Si on SiGe epilayer has about 10^5 defects/cm^2. Therefore compromises have been made to achieve a much lower level of strain-Si by other techniques such as localized strain-Si by STI formation, layered CVD oxide deposition or a few percent Ge implantation for example.

Vertical & Lateral Source Drain Engineering & Contact Formation Evolution

SDE and deep S/D. Current transistor designs use separate shallow SDE junction and deep S/D contacting junction implants and masks as illustrated in Fig. 10 (19,33). The optimization of SDE vertical junction depth (Xj) and lateral junction depth (Yj) called gate overlap/under diffusion and lateral abruptness in order to maximize device drive current is illustrated in Figs. 11 for under-diffusion and lateral abruptness optimization and in Fig. 12 for SDE and single-S/D junction depth optimization (30, 18). To control the SDE gate overlap precisely, off-set spacers are becoming standard at 90nm and beyond for both bulk and SOI devices (34, 35). Fig. 13 shows as updated roadmap for the most advanced logic devices taken from data reported in the ITRS-2001 and combined with the most resent customer inputs (1, 30, 36). For HP logic devices using oxynitride gate dielectric with poly electrode, high temperature dopant activation

annealing can be used for the SDE, deep S/D and poly gate doping activation and diffusion (37). However, starting at the 90nm node, the ultra shallow junction (USJ) requirements for SDE necessitates diffusion-less dopant activation annealing at either high temperatures or low temperatures while the deep S/D and poly gate doping will still require some dopant diffusion. Therefore, from a process integration point of view several companies will adopt the disposable spacer processing for SDE allowing the use of traditional high temperature spike/RTA annealing with dopant diffusion for the deep S/D and gate poly doping followed by either high temperature Flash annealing or low temperature SPE (solid phase epitaxy) annealing for diffusion-less dopant activation to achieve shallow and abrupt SDE junctions with gate overlap control as shown in the roadmap in Fig. 13 (37-39). For low power logic devices using high-k gate dielectrics and metal electrodes, low temperature dopant activation techniques will be required to prevent crystallization of the amorphous high-k gate material (37). Fortunately, the acceptable levels of junction leakage current for HP and LOP logic devices are within the acceptable range observed with low temperature SPE diffusion-less annealing (1, 37, 40). LSTP logic devices may require a combination of low temperature SPE annealing first followed by high temperature Flash annealing to further improve junction leakage at the expense of low Rs (sheet resistance). Further improvements in device performance can also be achieved with single-S/D as shown in Fig. 12 with the merging of the shallow SDE junction and deep S/D contact junction into a single junction with junction scaling as reported by Ozterk et al. shown in Fig. 10 (19). Single-S/D structures will require the use of elevated S/D contacting structures in order to achieve low S/D parasitic resistance and good silicide contacting just as SOI devices at 90nm and beyond with thin SOI <50nm thick now requires elevated S/D structures. For this reason single-S/D structures will first be implemented in SOI technology while bulk non-SOI devices will still require deep S/D to maintain low S/D parasitic resistance and good silicide contacting. Some companies have proposed a third deeper contacting junction for bulk CMOS devices (41, 42). Once bulk CMOS devices switch to elevated S/D then they too could merge the deep and shallow S/D junctions forming single-S/D.

<u>Single-S/D.</u> A simple way to transition from separate shallow SDE and deep S/D junction structures to a single-S/D structure is by using multiple high tilt implantation through the off-set spacer to form lateral graded SDE (LG-SDE) or single S/D (LG-SS/D) in either terraced shape (multi-mode implant) or wedged shape (rotation-mode implant) as shown in Fig. 14 (7). On one side of the gate stack structure the high tilt will implant the SDE or S/D dopant through the off-set spacer to achieve the desired gate overlap dopant encroachment. The other side of the gate stack structure will shadow the high tilt implant placing the dopant precisely at a distance away from the gate edge for the deeper contacting junction independent of the side wall spacer thickness control. Rotating the wafer for multiple twist implants ie. 4 to 8 rotations for a given tilt will create a terraced or wedged lateral structure as shown in Fig. 15 (7). Since the tilted implant is done through the off-set spacer the integration of this process can result in 2 mask savings with elevated S/D in SOI or bulk technology (Fig. 16) or when using a disposable spacer process flow that requires deep S/D for bulk contacting (Fig.17). Rotating the wafer from 0 degree orient/twist (A) to 45 degree twist (B) will also affect the lateral graded structure illustrated in Fig. 16 forming a triple LG-SDE (A) at 0 twist to a double LG-SDE (B) with a 45 degree twist using quad-mode implantation. If both 0 and 45 degree oriented transistors are present then an octa/8-mode implant (A+B) will be needed resulting in a penta/5-layered terraced LG-SDE structure. Conceptually, the

potential device benefits of the LG-SDE and LG-SS/D terraced or wedged structure are: 1) improved gate overlap control and SCE due to shallower Xj, more Yj and good lateral abruptness, 2) reduction in HALO dose so no channel mobility degradation and thereby delaying the need for strained-Si channel technology, 3) reduced gate overlap capacitance and junction capacitance and 4) improved Idsat and increased ring oscillator speed due to lower Rext (31). If using elevated S/D structures then a selective poly deposition process is preferred over a selective epi deposition process to avoid issues with side wall faceting control and interface surface cleaning sensitivity. This can be achieved using controlled interface cleaning with selective HF vapor etching (43, 44).

Elevated S/D. As mentioned earlier, elevated S/D will first be used at 90nm node with PD/SOI devices due to shallow S/D formation on thin silicon SOI layers of <50nm. As the deep S/D on bulk CMOS devices scale below 40nm junction depth it will also adopt elevated S/D at Lg between 20 and 40nm. Important to note is that the selective silicon (epi or poly) deposited structure does not have to be doped provided the silicide contact metalization process step completely consumes the planar facet free elevated silicon structure (43, 45-47).

Contacting Silicide: To reduce both contact and gate resistance the salicide process has evolved from TiSi2 to pre-amorphization TiSi2 to the current CoSi2 process. In the near future it will migrate to NiSi in order to further reduce poly gate resistance (2). To achieve good contacting a certain amount of silicon must be consumed. With SOI devices contacting becomes more problematic where the S/D parasitic resistance increases as the thickness of the SOI layer is reduced due to the higher resistance of the thin junction layer under the silicide layer preventing the current to spread and small interface contact area, therefore the need for elevated S/D (13, 16).

Novel SG Device Structure

Asymmetrical Transistor: For several years now asymmetrical transistors have been used by at least 6 companies in memory device applications around the world (36). They were fabricated using asymmetrical HALO implants because only medium current implanters were capable of the high tilt implant required and would take several hours to do the higher dose asymmetrical SDE implant (48). With the introduction of single wafer high tilt high current implanter with 60 degree tilt capabilities (VIISta-80), it is now possible to fabricate asymmetrical SDE devices as reported by Ghani et al. thus allowing further Lg channel scaling (49). Their results showed the importance of a minimal SDE gate under diffusion (overlap) value on the source side compared to the drain side on device performance.

Flash Memory Source Rail. Another unique application of high tilt high current implantation is for NOR flash memory source rail doping along the STI structure as reported by Song et al., (50). Using high tilt high dose implantation they obtained 25% lower source rail resistance in the trench topography. Today at least 8 flash memory companies are using self-align source line (SAS) with STI doping in manufacturing (36).

Vertical SG CMOS. As mentioned earlier, DRAM trench capacitor cell designs will remain on bulk silicon (non-SOI regions) and will evolve from planar SG to vertical SG transistors in order to scale the cell size down to sub-$8F^2$ for 16Gb generation as shown earlier in Fig. 2 (3). Tilted angle implantation and/or plasma implantation can

provide unique alternative 3-D doping capabilities for DRAM trench capacitor and stack capacitor cell designs. This vertical SG transistor design for DRAMs can also be used for embedded DRAM SOC with SOI logic devices using selective/patterned SOI wafers as reported by Sadana using patterned implanted SIMOX wafers and by Yamada et al. using selective epi on bonded SOI wafers shown earlier in Fig.6 (5, 6).

DOUBLE-GATE & MULTI-GATE CMOS

With expected difficulties in future scaling of single-gate FD/SOI CMOS devices the IC industry is looking at double-gate FD/SOI devices initially as a promising niche application alternative at Lg<20nm for the sub-45nm technology node. The silicon channel thickness in a DG FD/SOI transistor (0.75-0.5x Lg) must be thin enough to realize fully depleted channels for both gate structures and therefore expected to be thicker than SG FD/SOI (0.2-0.3x Lg) and therefore better SOI wafer manufacturing scalability (4). For MG FD/SOI the thickness now becomes equal to Lg. Other benefits include undoped to lightly doped channel so no mobility degradation and easing the concern of random dopant flucation effects, better SCE control and higher device drive currents. Also, lateral S/D dopant engineering and contact formation technique will be used for DG & MG novel devices as described earlier for the SG device architectures.

Planar (Top/Bottom) DG CMOS

In the planar DG structure one of the most difficult challenges and therefore critical requirements is the alignment of the top gate to the bottom gate (4). The simplest method is using wafer bonding techniques but here gate alignment is most difficult. Using multiple high tilt implantation the LG-SDE or LG-SS/D structure can also be formed for the planar DG structure as shown in Fig. 18 (7). Another approach is to use selective epitaxy with lateral growth through a tunnel to form first the source, then channel (tunnel) and lastly the drain. For this structure no SOI starting wafer is needed but this is a complicated structure to achieve and the lateral channel-S/D doping profiles for HALO, SDE & S/D are not realized using ion implantation.

FIN-FET DG & MG CMOS

The FIN-FET DG structure is the easiest to fabricate and thus currently the most popular DG structure found in the literature. For the FIN-FET design, the SOI silicon film thickness determines the minimum gate width (Wg) dimension so thicker SOI layers are required. With this structure, high tilt implantation up to 45 degree tilt for SDE and S/D prior to elevated S/D for improved salicide contacting will be required as reported by Kedzierski et al. (14). Additional flexibility for designing asymmetrical n+/p+ poly gate by high tilt poly gate implant doping is another option in transistor design for undoped channels as shown in Fig. 19 (14). If Wg is scaled down to equal Lg then a triple/multiple-gate structure can easily be realized as reported by Chau et al. of Intel (51). Again, multiple high tilt implantation for LG-SDE and LG-SS/D structures can be used with the various FIN-FET device structures. To create devices with various gate width, multi-FIN structures will be required (15).

Vertical Pillar DG CMOS

For the pillar DG design also called Vertical Gate Replacement (VGR) transistor an SOI wafer is also not necessary and the S/D, SDE and channel regions are selective epitaxially grown and doped (4). With the replacement gate process, high-k gate

dielectric can be designed but HALOs are not possible and the SDE is formed by dopant diffusion from doped oxide spacers. If the gate structure goes completely around the pillar or planar DG structure you get a quadruple-gate called gate all around or surround gate as shown in Fig. 3 (4).

SUMMARY

Multiple types of transistor designs and silicon wafers will be used as we continue to scale devices to meet the multitude of SOC applications in the future. Various 300mm wafer types including bulk CZ, epi, SOI and patterned SOI wafers will be necessary to accommodate planar and vertical SG as well as MG CMOS novel device structures. One key factor in extending SG designs and realizing DG/MG devices will be the use of flexible and uniform tilt angle ion implantation for precise dopant placement in 3-D (both vertically and laterally) for novel device structures.

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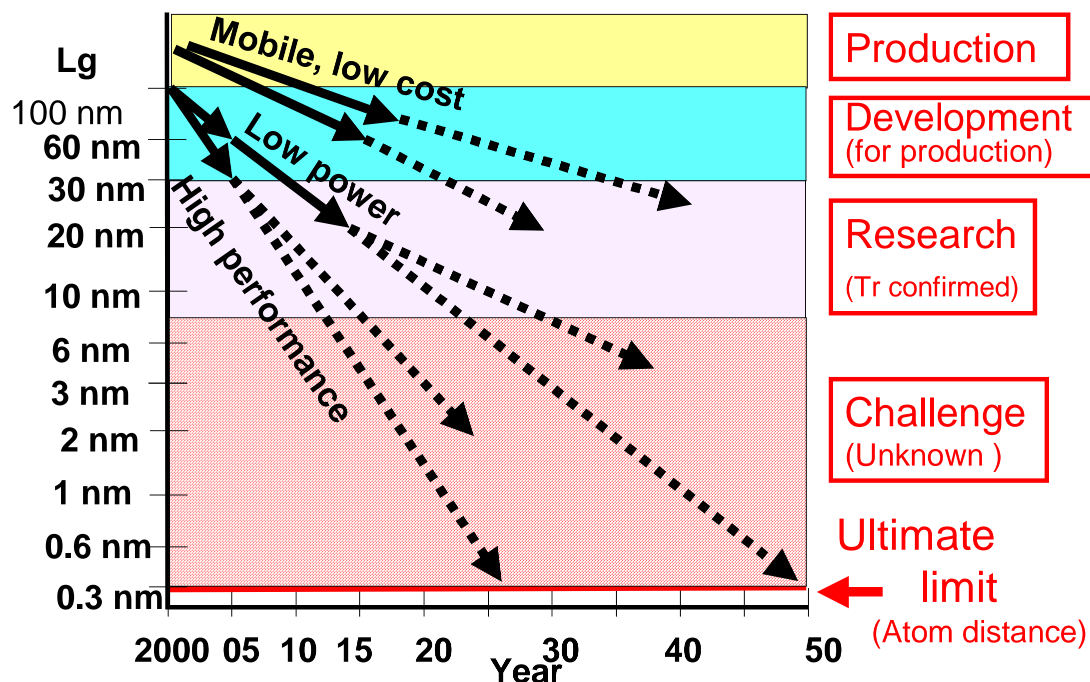

Fig.1: Multiple (HP, LOP & LSTP) logic device roadmaps (2).

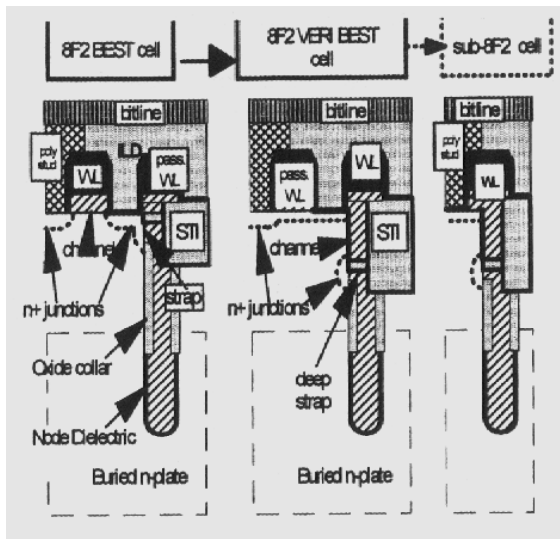

Fig.2: Evolution from planar to vertical SG transistor for DRAM (3).

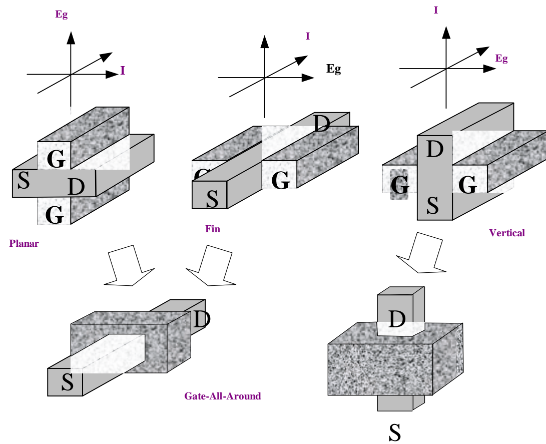

Fig.3: Evolution from SG to various DG & MG transistor designs (4).

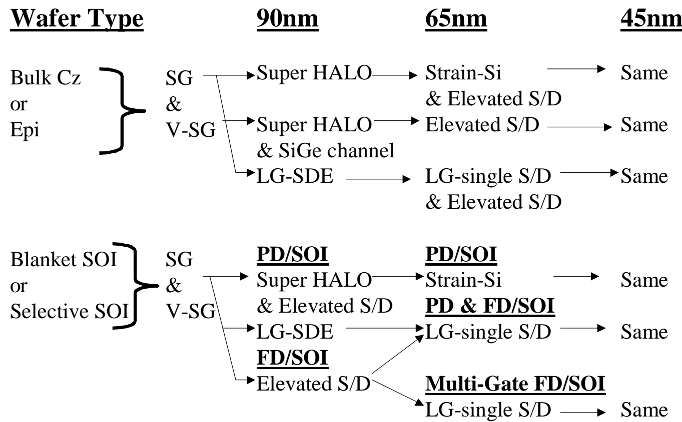

Fig.4: Wafer, transistor & novel device structure evolution.

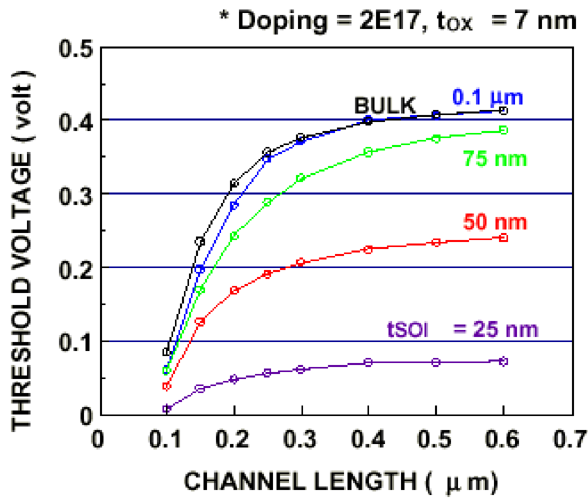

Fig.5: SOI film thickness sensitivity on Vt and SCE (17).

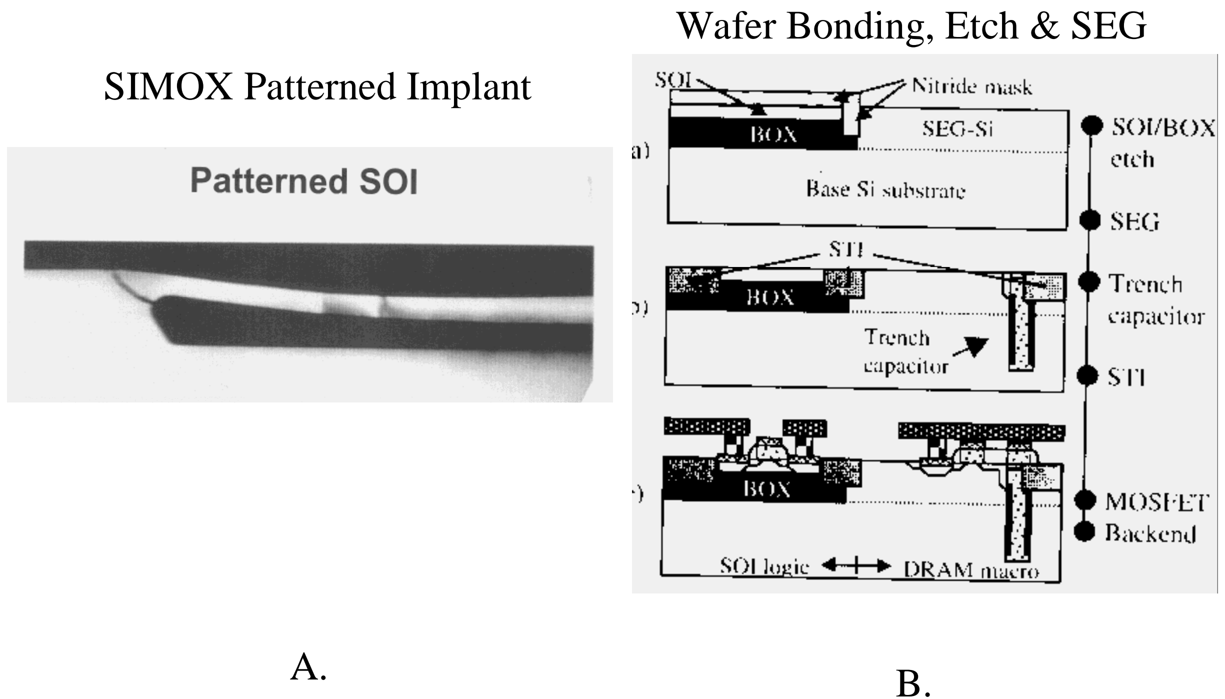

Fig.6a&b: Selective/patterned SOI wafer for embedded/SOC (5,6).

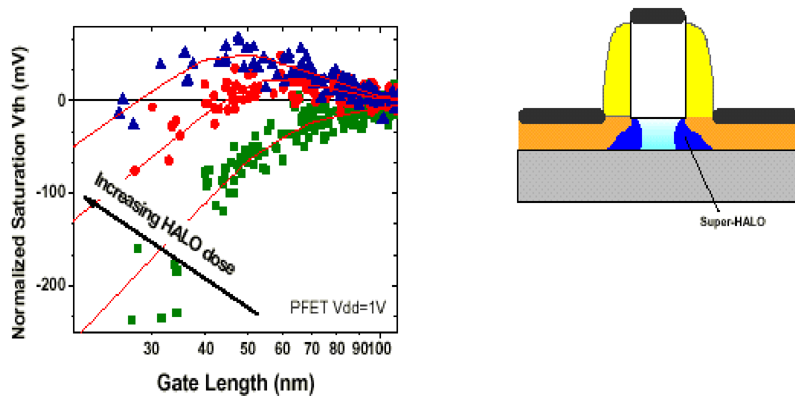

Fig.7: Super HALO for PD/SOI (17).

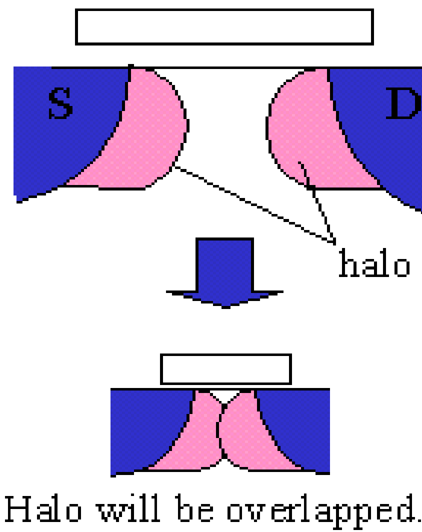

Fig. 8: HALO overlap for narrow Lg (2).

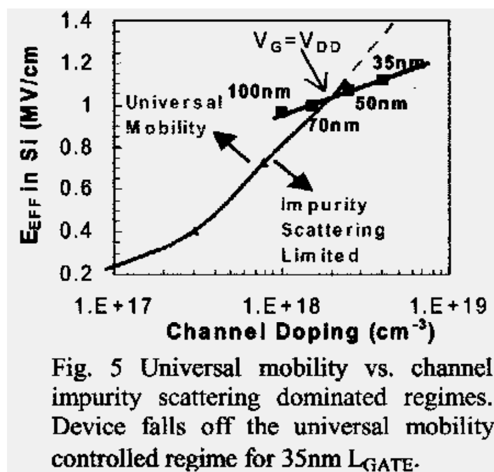

Fig. 5 Universal mobility vs. channel impurity scattering dominated regimes. Device falls off the universal mobility controlled regime for 35nm L_{GATE}.

Fig.9: Channel doping concentration effects on mobility (30).

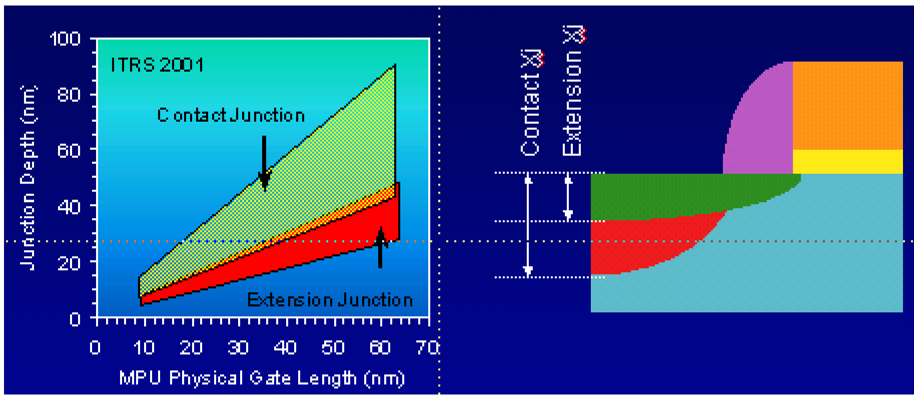

Fig.10: Merging SDE and deep S/D into single junction (19).

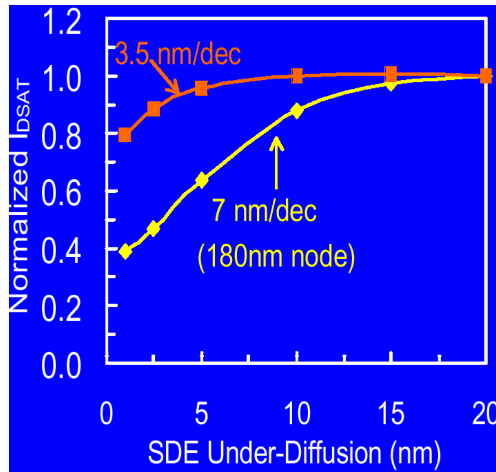

Fig.11: Lateral abruptness and gate overlap optimization (30).

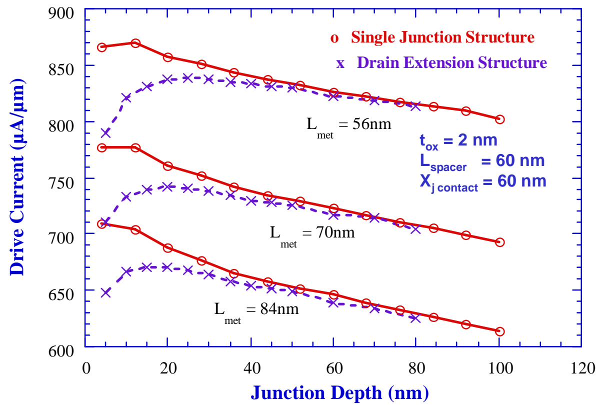

Fig.12: SDE and single S/D junction depth optimization (18).

Year	2001	2003	2005	2007	2009	2011	2013	2015
Node (nm)	130	90	65	45	32	23	16	11
Lgate (nm)	70	50	35	25	18	13	9	6
Wafer size (mm)	200	300	300	300	300	450	450	450
EOT (nm)	1.5	1.2	0.8	0.6	0.5	0.45	0.4	0.3
SDE Xj (nm)	35	24	17	12	8.5	6.0	4.2	3.0
SDE Rs (ohms/sq.)	400	550	830	830	940	1015		
SDE (dopant/cm3)	5E19	8E19	1.0E20	1.5E20	2.0E20	2.5E20		
SDE Yj (nm)	16	11	8	5.6	4	2.8	<2	
Abruptness (nm/dec)	7.2	4.1	2.8	2	1.4	1	<1	
HP-leakage (A/cm2)	15	100	1E3	5E3	1E4	2E4	6E4	1E5
LOP-leakage (A/cm2)	1	1.5	2	5	10	20	50	100
LSTP-leakage (A/cm2)	1E-3	1.5E-3	2E-3	5E-3	1E-2	2E-2	5E-2	0.10

Fig. 13: Updated roadmap targets for advanced logic devices.

New Multiple High Tilt Implant (Quad-mode or Rotation)

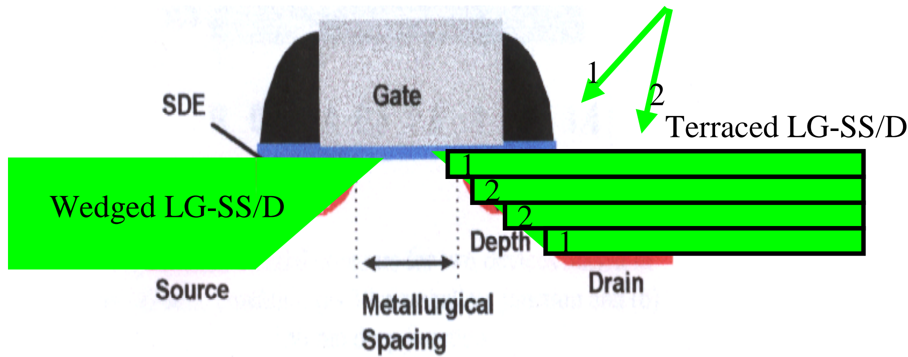

Fig.14: LG-SS/D wedged or terraced shaped structure using multiple high tilt implantation (7).

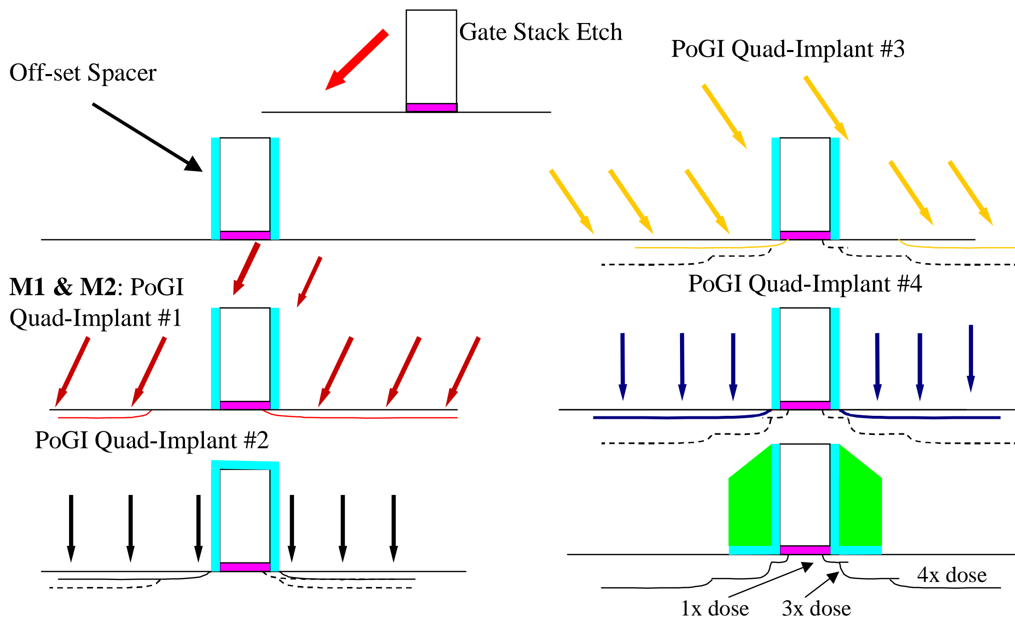

Fig.15: PoGI high tilt quad-mode multiple implantation to form LG-SDE or LG-SS/D terraced or wedged shape structure (7).

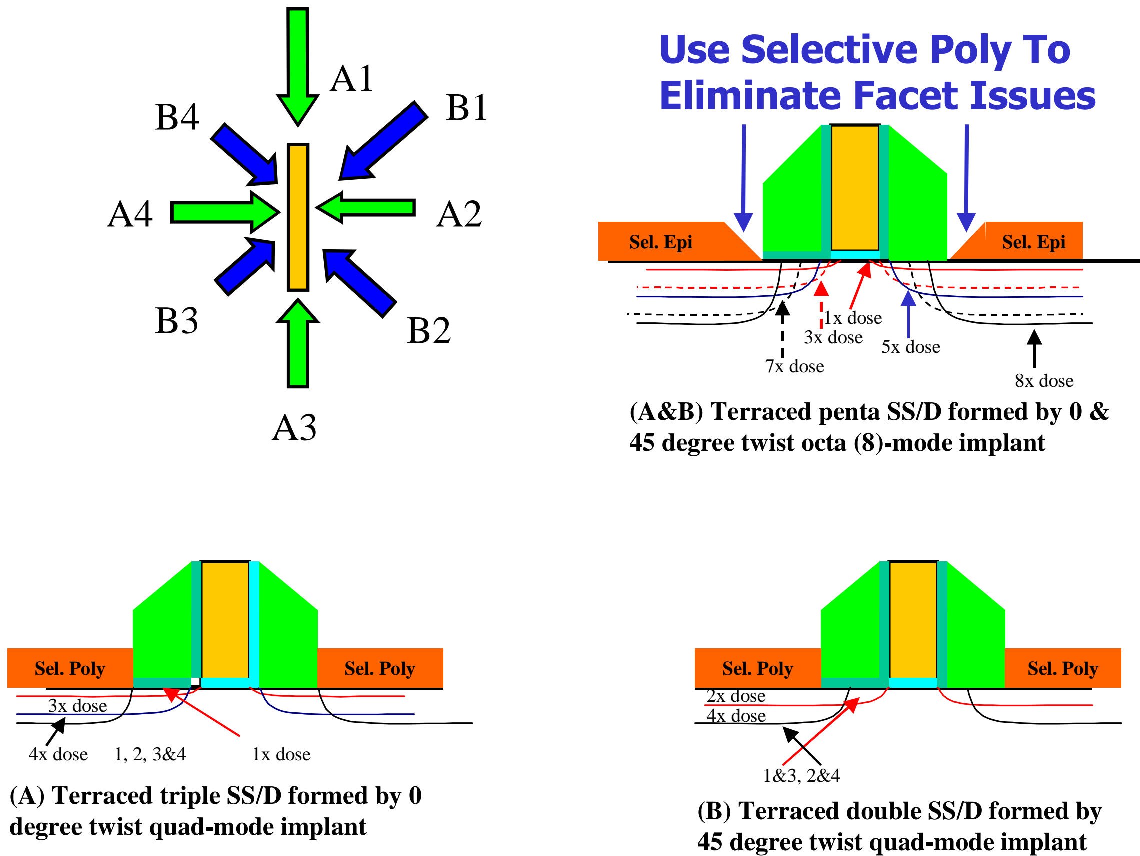

Fig.16: Elevated S/D (epi or poly) and wafer orient/twist effects on the LG-SS/D structure (7).

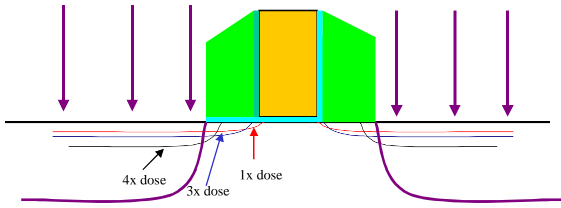

Fig. 17: LG-SDE with separate deep S/D contacting implant (7).

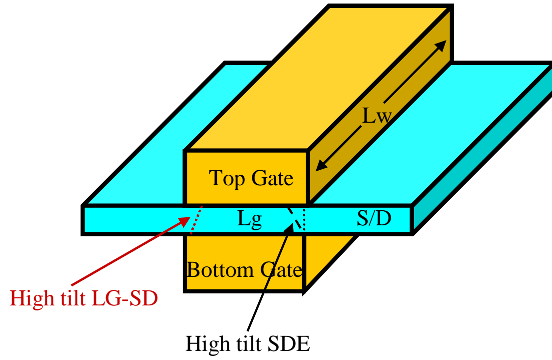

Fig. 18: Planar DG with LG-SS/D or LG-SDE (7).

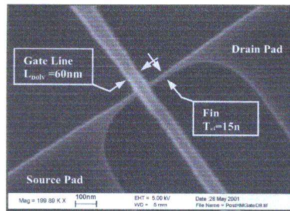

Figure 2: Top Down SEM, of a <110> SDG FinFET device after gate and hardmask etch. Device measurements: Tsi = 15nm, Lpoly = 60nm.

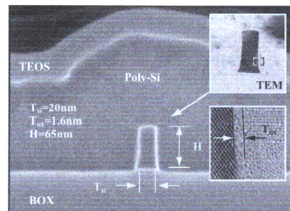

Figure 3: Xsection of a <110> SDG FinFET perpendicular to current flow. Measurements: Tsi = 20nm, Tox = 1.6nm, Tpoly=150nm W=130nm (2x Fin Height). Inset shows TEM of fin and gate oxide.

ADG
n+ & p+
poly gate

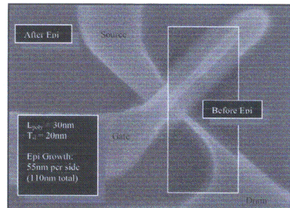

Figure 4: Top Down SEM, of <100> SDG FinFET before and after selective Si epitaxy. Device measurements: Tsi = 20nm, Lpoly = 30nm.

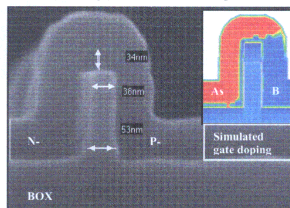

Figure 5: Xsection SEM of ADG NMOS FinFET perpendicular to current flow. Tsi=40nm, Tox=2.2nm, Tpoly=120nm, W=240nm (2x Fin Height). Inset shows the simulated doping profile after extension implant.

Fig.19: FIN-FET with asymmetrically doped DG (n+ & p+) (14).