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## Shallow and abrupt junction formation:

# Paradigm shift at 65-70nm

**OVERVIEW** The low-temperature (550–750°C) solid phase epitaxial method of forming shallow junctions is an attractive activation technique for the 65–70nm node and beyond. This novel method can be easily integrated into devices that are formed using a disposable spacer, or into low power CMOS devices using high-*k* dielectrics.

With the continued growth trends in portable devices — along with their precursors, desktop computers — more and more emphasis is being placed on improving low power CMOS devices. This is driving the switch from oxynitride-type gate dielectrics with polysilicon electrodes, to high-*k* ($HfO_2$) dielectrics with metal electrodes by 2005, to satisfy the sub-90nm technology node.

High-*k* dielectric materials have demonstrated orders of magnitude reduction in gate leakage with super thin equivalent gate oxide thicknesses. Their control and deposition processes, however, are still very immature and thus the focus of development at consortia such as International-SEMATECH and Selete (Semiconductor Leading Edge Technologies, Ltd.). However, thermal stability and thermal resistance properties at elevated (high) temperatures above 700°C are fundamental material issues for high-*k* dielectrics and metal electrodes. Several groups have reported that the thermal stability of amorphous high-*k* dielectrics is limited to <700°C for $HfO_2$ and <800°C for $ZrO_2$ before recrystalization occurs, degrading the dielectric constant, as reported by Niwa [1].

Selection of the metal electrode material can also impose thermal budget limitations. To avoid such constraints in the formation of shallow junctions, a replacement gate process scheme was proposed several years ago. Unfortunately, it proved very difficult to manufacture and was abandoned by most [2, 3]. Osburn of NCSU reported the replacement gate process adds 2+ masking levels and 20% more processing steps [2]. Others have reported on a key-hole structure resulting from the metal electrode deposition process due to the narrow aspect ratio [3]. Also, difficulty in precleaning the silicon surface prior to high-*k* dielectric deposition has been reported. This difficulty becomes even more problematic in the replacement gate structure that contains the narrow and steep sidewall geometries of the removable dummy gate structure.

Thus, with a conventional gate stack formation scheme for high-*k* dielectric with metal electrodes, the ion implanted shallow junction formation process will require a paradigm shift from high-temperature annealing (>1000°C) to low-temperature annealing (<700°C) for dopant activation and defect location engineered annealing for both source drain extension (SDE) and deep source drain formation. For these reasons, there are now numerous groups around the world that are investigating low-temperature solid phase epitaxial (SPE) regrowth in detail. These groups are also implanting amorphous shallow junction structures using various beam-line and plasma dopant species with a variety of pre-amorphizing implant (PAI) conditions in the temperature range of 550–700°C. These results are summarized in Table 1, showing the compatibility of the annealing techniques with high-*k* gate stack structures for shallow junction formation.

### Shallow and abrupt junction roadmap

The SDE shallow junction requirements based on the 2001 ITRS Roadmap are listed in Table 2 [4]. Vertical junction depth ($X_j$), sheet resistance ($R_s$), and lateral abruptness targets are identified for each technology node. For the 65–70nm node, the target for $X_j$ is 10–19nm, $R_s$ is 760–830Ω/sq, and abruptness is 2.8–3.1nm/decade. Another key SDE parameter not identified in the 2001 roadmap is the critical lateral gate overlap value, which is the amount of SDE diffusion under the gate edge. Ghani, et al., from Intel, reported CMOS scaling projections of transistor parameters (Table 3) for the critical SDE shallow junction for both vertical $X_j$ and lateral $Y_j$ gate overlap dimensions [5]. In this paper, it is shown that reducing gate overlap degrades IDSAT, but improving lateral junction abruptness from 7nm/decade down to 1.5nm/dec improves it. For their technology at 180nm, a 7nm/dec lateral abruptness required a minimum gate overlap >20nm, while for a 3.5nm/dec lateral abruptness, the minimum gate overlap could be reduced to >7.5nm.

Similarly, it has been reported that, for extreme abruptness, a <1.0nm/dec negative gate overlap (gate underlap) of <5.0nm is desir-

**Table 1 USJ activation methods for high-*k* gate application**

| Initial USJ anneal condition | Additional high-temp. effects |
|---|---|
| Green = can achieve attribute; Blue = attribute is marginally affected; Red = cannot achieve attribute | |
| **High-temp flash anneal** | **High-temp flash anneal** |
| Low temperature <700°C | Not applicable (N/A) |
| Shallow junction | N/A |
| Low $R_s$ | N/A |
| Low junction leakage | N/A |
| **High-temp laser-melt anneal** | **HT laser-melt anneal + RTA** |
| Low temperature <700°C | Low temperature <700°C |
| Shallow junction | Shallow junction |
| Low $R_s$ | Low $R_s$ |
| Low junction leakage | Low junction leakage |
| **Low-temp SPE anneal** | **Low-temp SPE anneal +RTA** |
| Low temperature <700°C | Low temperature <700°C |
| Shallow junction | Shallow junction |
| Low $R_s$ | Low $R_s$ |
| Low junction leakage | Low junction leakage |

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**Table 2** 2001 ITRS for USJ (SDE) [4] Solution: exists (white); being pursued (yellow); and not known (red)

| Year of production | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 | 2010 | 2013 | 2016 |
|---|---|---|---|---|---|---|---|---|---|---|
| DRAM 1/2 pitch (nm) | 130 | 115 | 100 | 90 | 80 | 70 | 65 | 45 | 32 | 22 |
| MPU/ASIC 1/2 pitch (nm) | 150 | 130 | 107 | 90 | 80 | 70 | 65 | 50 | 35 | 25 |
| MPU gate length (nm) | | | | | | | | | | |
| printed | 90 | 75 | 65 | 53 | 45 | 40 | 35 | 25 | 18 | 13 |
| physical | **65** | **53** | **45** | **37** | **32** | **28** | **25** | **18** | **13** | **9** |
| Equivalent physical oxide thickness for MPU/ASIC Tox (nm) | 1.3–1.6 | 1.2–1.5 | 1.1–1.6 | 0.9–1.4 | 0.8–1.3 | 0.7–1.2 | 0.6–1.1 | 0.5–0.8 | 0.4–0.6 | 0.4–0.5 |
| Gate electrode thickness (nm) | 65–130 | 53–106 | 45–90 | 37–74 | 32–64 | 30–60 | 25–50 | 18–36 | 13–26 | 9–18 |
| Profile control (side wall angle) | >89 | >89 | >89 | 90 | 90 | 90 | 90 | 90 | 90 | 90 |
| Drain exten. $X_j$ (nm) | 27–45 | 22–36 | 19–31 | 15–25 | 13–22 | 12–19 | 10–17 | 7–12 | 5–9 | 4–6 |
| Max. drain extension $R_s$ (PMOS) (Ω/sq) | 400 | 460 | 550 | 660 | 770 | 830 | 760 | 830 | 940 | 1210 |
| Extension lateral abruptness (nm/decade) | 7.2 | 5.80 | 5.0 | 4.1 | 3.5 | 3.1 | 2.8 | 2.0 | 1.4 | 1.0 |

able, although with a 6.4nm/dec, a minimum gate overlap of >6.0nm is desired [6]. It has been found that reducing gate overlap improves short channel effects (SCE) and gate channel length ($L_{eff}$) for bulk CMOS and SOI-CMOS [7]. The insertion point for devices — high-*k* gate with metal electrodes in 2006 for the 65–70nm node low power CMOS devices, and 2010 for the 45–50nm high performance MPU CMOS devices — will have an impact on the USJ (ultra shallow junction) roadmap for dopant and activation method based on gate stack structure (Fig. 1) [8].

**Table 3** Scaling projection of transistor parameters for future logic technology generations

| Generation (nm) | 180 | 130 | 100 | 70 | Scaling factor |
|---|---|---|---|---|---|
| SDE depth (nm) | 50 | 35 | 24 | 17 | 0.7× |
| SDE under-diff (nm) | 23 | 16 | 11 | 8 | 0.7× |
| $L_{MET}$(nm) | 55 | 40 | 27 | 20 | 0.7× |

Source: Ghani, et al., Intel, VLSI Symposium, June 2000

The emergence of the high-*k*/metal gate stack structure option in 2006 with low-temperature dopant activation methods and a new plasma doping method is important to note. Also, sometime after 2006, elevated source/drain structures will enter the scene; this will be especially relevant for thin SOI layers <50nm thick, where low salicide source drain contact resistance is critical. This includes both partially depleted and fully depleted SOI devices [9]. Elevated source drain structures will also benefit the move to single drain technology [10, 11]. The universal $R_s$ vs. $X_j$ chart with technology node windows and boron dopant activation levels (solid solubility limits) for a box profile first created by Shishiguchi of NEC and modified by Osburn of NCSU, Muto of I-SEMATECH, and Borland of VSEA, is shown in Fig. 2 [11–14]. From this chart, it can be seen that the 100nm node requires box profile boron dopant levels around 8E19/cm$^3$; the 70nm node, around 1E20/cm$^3$; the 50nm node, about 1.5E20/cm$^3$; the 35nm node, about 2E20/cm$^3$; and the 25nm node, around 2.5E20/cm$^3$.

Note the dramatic change between the 1999 and 2001 ITRS targeted SDE $R_s$ values. These new, relaxed requirements are more realistic and based on 12% of the total series resistance targets. They now agree with the device simulation analysis for SDE reported two years ago. S. Kim, et al., of UCLA, H. Gossmann, et al., of Bell Labs/Agere, and Y. Taur of IBM, published dissenting opinions of the 1999 ITRS SDE $R_s$ targets [15–17].

### High-temperature RTA spike/flash (non-melt) annealing

The most advanced annealing technique in state-of-the-art, 130nm production manufacturing is rapid thermal anneal (RTA) spike annealing with controlled oxygen to reduce oxidation enhanced diffusion (OED). Using beam-line implantation at energies down to 500eV in decel mode for $B_{11}$ or 2keV for $BF_2$ at a dose of 1E15/cm$^2$ and <0.3% energy contamination, one can achieve a <22.0nm as-implanted $X_j$ defined at 1E18/cm$^3$. If using drift mode, such as implantation conditions with <0.05% energy contamination, then a 14.3nm as-implanted $X_j$ and abruptness of 2.7nm/dec is achieved [8].

Development for 90–100nm technology is being done at energies as low as 200eV in decel mode for $B_{11}$ and 1keV for $BF_2$ with 0.3% energy contamination to achieve as-implanted $X_j$ <18.0nm. For 65–70nm R&D

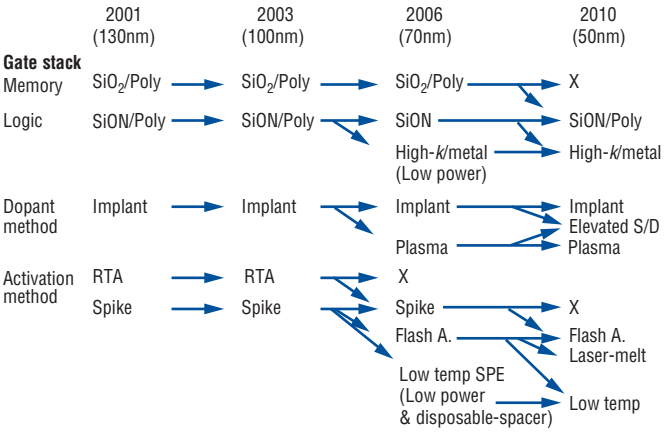


**Figure 1.** USJ roadmap alternatives based on gate stack structure.

development, drift mode implantation with no detectable energy contamination (<0.05%) at 200eV for $B_{11}$ is being used to achieve 9.0nm as-implanted $X_j$ value at 1E18/cm$^3$ level with 2.1nm/decade abruptness [10]. At these implant conditions, very low beam current is realized, raising concerns for production viability. Using $BF_2$ instead allows higher implant energies and beam currents, but there are reported concerns with F impurity affecting $SiO_2$ gate oxide quality [18]. However, $BF_2$ implantation can be extended through optimized oxynitride gate dielectric material [19].

Another option is to replace beam-line implantation with plasma implantation at slightly higher energies than $B_{11}$ but with higher beam current and 2–3× higher productivity. Figure 3 shows a collection of boron SDE as-implanted results showing junction depth vs. implant energies for plasma $BF_3$ and beam-line $B_{11}$ and $BF_2$. Also shown are values with <0.05% or <0.3% energy contamination. The industry will be rapidly approaching the lower energy limit of beam-line $B_{11}$ implantation at the

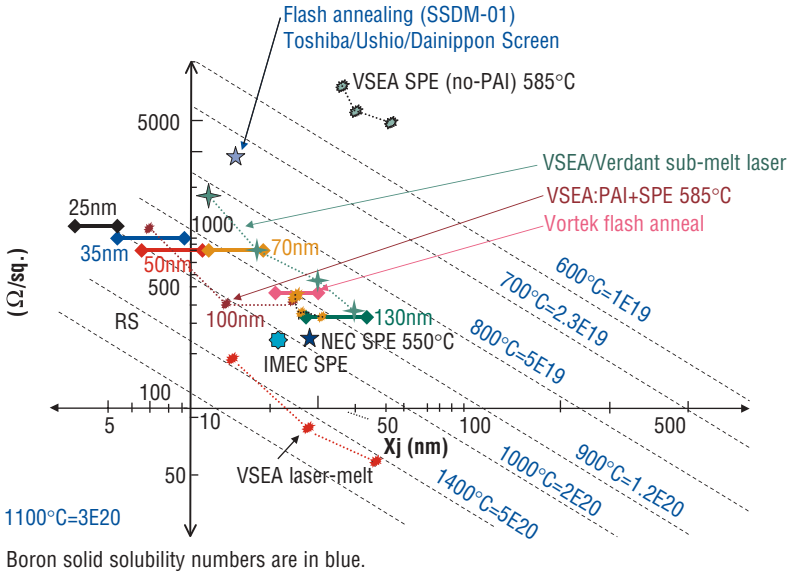


**Figure 2.** $R_s$ vs. $X_j$ for various activation methods.

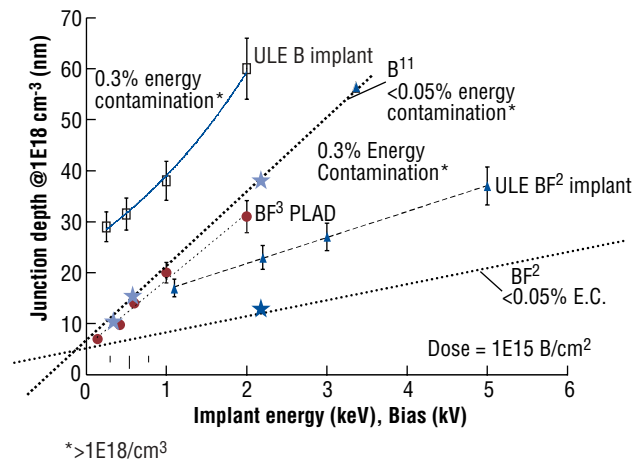


**Figure 3.** Boron as-implanted junction depth vs. implant energy defined at 1E18/cm$^3$.

65–70nm node.

Optimizing high-temperature RTA annealing conditions, however, can significantly impact $X_j$. The benefits of PAI on reducing transient enhanced diffusion (TED) for $B_{11}$ implants >1keV [11], the influence of controlled oxygen ambient during RTA processing to reduce oxidation enhanced diffusion (OED) [20], and ramp rate effects [20, 21] have been shown. For example, sub-keV $B_{11}$ implants and high ramp-up and cool-down rates have been reported to reduce $X_j$, while controlled oxygen showed minimal effects for sub-keV implants. Also, sub-keV $B_{11}$ implants using PAI of Si or Ge with RTA spike annealing produced deeper junctions, though as-implanted profiles were shallower with PAI due to the elimination of channeling. Sub-keV $B_{11}$ implants show a surface dose sputtering limit as the energy is reduced below 500eV, and the dose is increased above 2E15/cm$^2$ [22].

Ion implantation shallow junction formation by high-temperature (>1000°C) RTA spike, flash or sub-melt laser annealing with oxide or oxynitride/polysilicon electrode gate stack structures, should be extendable down to the 65–70nm technology node (2006). Additionally, it should be limited to <2E20/cm$^3$. In reality, however, it is limited to <8E19/cm$^3$ boron electrically active dopant level due to the boron solid solubility limit in silicon, therefore, it's equivalent to the 100nm technology node requirement (2003). Table 4a summarizes the best high-temperature (1050°C) RTA spike annealing results — assuming an average of +8.0nm dopant diffusion from the as-implanted profile. The limiter to this annealing methodology at the 100nm technology node is not implant energy, but rather fundamental dopant activation, which seems to be at a level of <8E19/cm$^3$ for boron in silicon corresponding to an equilibrium temperature of <900°C as shown earlier in Fig. 2. Implant energy becomes a limiter at the 70nm node (Table 4a).

To further reduce dopant diffusion/movement and maintain the as-implanted profile with abrupt junctions, super fast ramp-up and -down rate annealing techniques (flash annealing) have been proposed. In this process, the times are on the duration of milliseconds. Examples include arc-lamp annealing, sub-melt laser annealing, and, most recently, xenon lamp annealing [23–25]. At the SSDM-2001 meeting in Tokyo, studies using standard tungsten halogen lamps on an RTA system's bottom to first heat the wafer up to ~500°C were presented, and then, using xenon top lamps, to achieve flash annealing up to 1050°C in <30msec [25]. Using a 200eV $B_{11}$ implant, the researchers achieved $X_j$ = 15nm and $R_s$ = 3K Ω/sq. (Fig. 2), and stated this is their target at Toshiba for 70nm node devices [25]. Figure 2 also shows results from Vortek's arc lamp flash annealing and Verdant's laser non-melt flash annealing techniques. Note that the best high-temperature annealing result is still <1E20/cm$^3$, equivalent to the 900°C solid solubility limit of boron in silicon. Thus, at best, high-temperature flash annealing can satisfy only two of the four requirements for high-*k* USJ process integration (Table 1).

## High-temperature laser melt annealing

High-temperature laser annealing has been studied for over 25 years and led to the development of RTA lamp annealing in the early 1980s. Laser melt annealing in the 1200–1400°C temperature range has been recently studied and reported to have only achieved two out of the four shallow junction requirements (Table 1).

A review of the results with laser-melt annealing were presented at the Spring 2001 MRS meeting [26]. Device level integration issues with laser melting must be overcome before this technique will be accepted in manufacturing. The major challenges are: melting the silicon under the STI isolation oxide structure, which can result in the oxide structure pop-

**Table 4 Interpretation of the 2001 ITRS implant requirements**

| | 130nm | 100nm | 70nm | 50nm | 35nm |
|---|---|---|---|---|---|
| **Year** | **2001** | **2003** | **2006** | **2010** | **2013** |
| Xj (nm) | 27–45 | 19–31 | 12–19 | 7–12 | 5–9 |
| Rs | 400 | 550 | 830 | 830 | 940 |
| Dopant level/cm$^3$ | 5.00E+19 | 8.00E+19 | 1.00E+20 | 1.5E20 | 2E20 |
| **a) Based on high-temperature RTA/flash annealing<br>High-temperature RTA/spike $X_j$ = (As-implanted $X_j$ + 8nm)** | | | | | |
| Xj–8nm | (19–37) | (11–23) | (4–11) | (–1–4) | (–3–1) |
| Dose range | 0.5–1E15 | 0.5–1E15 | BSS | BSS | BSS |
| $B_{11}$ (0.3% E.C.) | <1keV | <100eV | – | – | – |
| (no E.C.) | 0.7–1.3keV | 300–800eV | <300eV | N/A | N/A |
| $BF_2$ | 1.9–4.8keV | 0.2–2.2keV | <200eV | N/A | N/A |
| (no E.C.) | 3.5–6.5keV | 1.5–4.0keV | <1.5keV | N/A | N/A |
| PLAD | 1.2–2.5kV | 0.4–1.7kV | <400V | N/A | N/A |
| **b) Based on high-temperature laser melt annealing<br>High-temperature laser thermal melting $X_j$ = Ge-PAI EOR depth** | | | | | |
| Dose range | 0.5–1E15 | <1E15 | <1E15 | <1E15 | <1E15 |
| Ge-PAI (keV) | 17–29 | 12–20 | 7–12 | 3–7 | 2–4.5 |
| $B_{11}$ (0.3% E.C.) | 0.5–1.3keV | <500eV | N/A | N/A | N/A |
| (no E.C.) | 1–1.7keV | 0.6–1.1keV | 300–600eV | 150–300eV | 80–200eV |
| $BF_2$ (0.3% E.C.) | 3–6.5keV | 1.8–3.7keV | 0.2–1.7keV | <200eV | N/A |
| (no E.C.) | 5–8.3keV | 3–5.5keV | 1.5–3keV | 0.75–1.5keV | 0.4–1keV |
| PLAD | 1.6–3kV | 1.2–2keV | 0.5–1.2kV | 200–600V | 100–300V |
| **c) Based on low-temperature SPE annealing<br>Low-temperature SPE $X_j$ = As-implanted junction depth** | | | | | |
| Dose range | 0.5–1E15 | 0.5–1E15 | 0.5–1E15 | 0.5–1E15 | 5.00E+15 |
| Ge-PAI (keV) or | 11–21 | 10–14 | 6–10 | 3–6 | 2.5–5 |
| Si-PAI (keV) | 9–16 | 7–10 | 4–7 | 2–4 | 2–3 |
| $B_{11}$ (0.3% E.C.) | 0.5–1.3keV | <500eV | N/A | N/A | N/A |
| (no E.C.) | 1–1.7keV | 0.6–1.1keV | 300–600eV | 150–300eV | 80–200eV |
| $BF_2$ (0.3% E.C.) | 3–6.5keV | 1.8–3.7keV | 0.2–1.7keV | <200eV | N/A |
| (no E.C.) | 5–8.3keV | 3–5.5keV | 1.5–3keV | 0.75–1.5keV | 0.4–1keV |
| PLAD | 1.6–3kV | 1.2–2keV | 0.5–1.2kV | 200–600V | 100–300V |

ping out; polysilicon gate stack electrode melting and rounding; and limiting lateral junction profile for gate overlap and leakage control due to the lateral extent of the PAI layer.

A key element to laser melt annealing is the location of the Ge-PAI layer, which defines the melt region and thus junction depth vertically and laterally. The Ge-PAI layer also lowers the melting temperature of silicon by 200°C, from 1400°C to 1200°C, and it creates end-of-range (EOR) damage that remains beyond the amorphous/crystalline silicon interface leading to poor junction leakage in both the vertical and lateral direction. To improve leakage, the junction must diffuse beyond the EOR damage, which can be achieved through an additional RTA anneal [26]. Using an additional 800°C, 20 sec RTA anneal after the laser melt annealing step, researchers were able to drive the junction an additional 15.0nm deeper, thus improving junction leakage. However, junction depth increased by 33%, from 45.0nm to 60.0nm.

Another negative impact of the RTA anneal (as described previously) on the laser annealed shallow junction, was the activation of transient enhanced diffusion (TED) and dopant deactivation (solid solubility limit) effects. Y. Takamura, et al., of Stanford, reported that post-laser melt annealing dopant deactivation in the 500–900°C temperature range occurs within the first 10 sec of an RTA anneal, and can result in up to 90% dopant deactivation [27]. Nevertheless, a high boron electrically active dopant level of 5E20/cm$^3$ immediately after laser melt annealing can be realized, thereby satisfying the sub-25nm technology node. The $R_s$ vs. $X_j$ results for laser melt annealing are shown in Fig. 2; the 5E20/cm$^3$ value agrees with the solid solubility limit of boron in silicon at the melting temperature of silicon (1400°C).

As noted above, process integration and material compatibility will limit the use of laser melt annealing. Also, post laser melt wafer thermal treatment results in dopant deactivation and solid solubility limit degradation in the $R_s$ value. Additionally, the need to improve junction leakage by driving the junction deeper, offsets all the advantages of laser melt annealing in the first place. High-*k* gate stack structures have a thermal limit of <700°C to prevent re-crystallization and dielectric constant degradation. Therefore, laser melting is not an option and its only potential application is limited to $SiO_2$ and SiON gate stack structures and it can be used through the sub-25nm technology node. Table 4b shows the interpretation of the 2001 ITRS roadmap with laser melt annealing extending ion implantation to the sub-50nm node where the limitation becomes implant energy below 200eV with production viable productivity. For these reasons, laser melt annealing has also been abandoned by a number of leading logic device manufacturing companies around the world [10].

## Low-temperature SPE annealing (550–750°C)

Low-temperature SPE annealing has also been investigated off-and-on over the last 20+ years, but in 2001, the need for a manufacturing solution when using high-

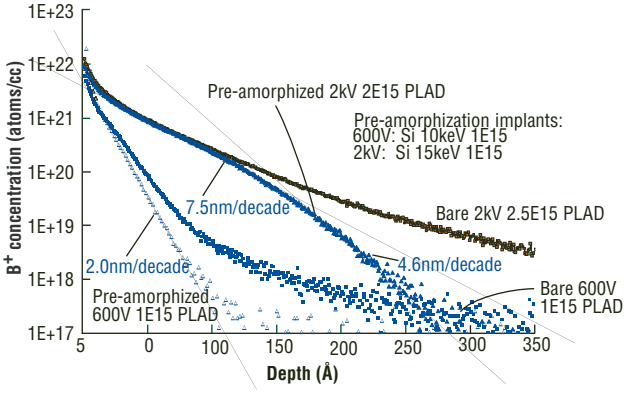


**Figure 4.** PAI for channeling elimination.

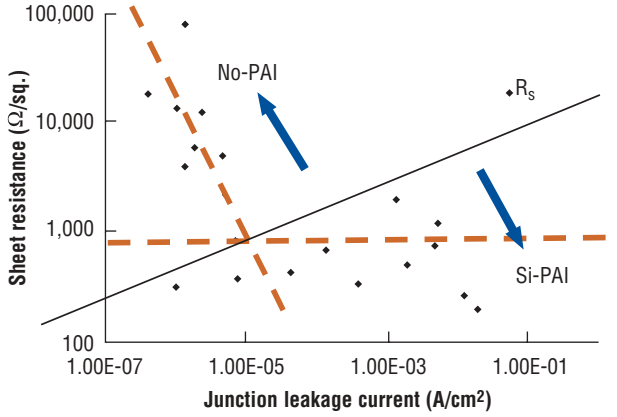


**Figure 5.** Low temperature SPE results for $R_s$ vs. junction leakage.

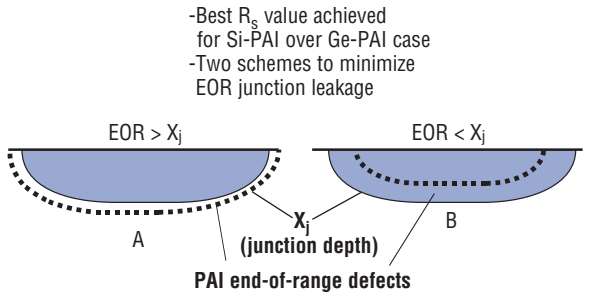


**Figure 6.** SPE leakage study for optimization of $X_j$ and PAI-EOR. Scheme A is preferred if the entire transistor formed within EOR. Scheme B is preferred if S/D, S/D ext, channel formed separately. Agere characterizing diode devices on both schemes. The University of Florida is doing TEM analysis; others will also test device leakage.

*k* gate stack structures created great interest once again in this technology. With SPE, all four of the requirements for high-*k* USJ process integration have been realized (Table 1). Currently, the main focus of the research on SPE is on optimizing an acceptable level of junction quality through PAI optimization. Nevertheless, the top logic manufacturers in the US, Japan, Taiwan, and Europe, are now developing low-temperature annealing processes for their 70nm technology driven by low power CMOS devices. These processes will use high-*k* gate stack structures [10]. At temperatures <750°C, no dopant diffusion is observed comparing temperatures from 750°C up to 1050°C [28]. Using a 500V $BF_3$ plasma implant, researchers showed that the as-implanted junction depth was 14nm. With a 750°C/10 sec anneal, no dopant diffusion was observed and junction depth was 14nm. With a 850°C/10sec anneal, the junction moved 8.5nm to a depth of 22.5nm. With a 950°C/10 sec anneal, the junction moved 23.5nm to a depth of 37.5nm. With a 1050°C/10sec anneal, the junction moved 66nm to a depth of 70nm.

Using PAI of Si or Ge eliminates channeling, resulting in very shallow and abrupt as-implanted junctions ($X_j$<8.0nm and <2.0nm/dec) as shown in Fig. 4 for 600V, and 2kV $BF_3$ plasma implantation. Note this was not the case with high-temperature RTA spike annealing as discussed earlier, where PAI resulted in deeper junctions after high-temperature annealing [11]. SPE re-crystallization rates as a function of temperature were reported by Jacobson, who observed the rate to be 0.1A/sec at 500°C, 1A/sec at 550°C, 10A/sec at 600°C, 100A/sec at 660°C, 1000A/sec at 730°C, and 10,000A/sec at 830°C [29]. At 600°C, 60nm of SPE occurs in 1 min. There have also been reports on dopant activation by SPE in the 450–650°C range.

Complete dopant activation was achieved in <5min at 580°C, where $R_s$ and uniformity for arsenic implant went from 190Ω/sq. and 25% nonuniformity after 3 min annealing to 37Ω/sq. and 17% uniformity after 5 min. After 7 min, it was 27Ω/sq. and 3% uniformity [30]. Similar SDE high dopant activation was reported with antimony SPE [31]. Low-temperature SPE results with the current dopant activation limit at the supersaturation level of 2.5E20/$cm^3$ for boron can be seen in Fig. 2. Applying SPE to the 2001 ITRS roadmap shows similar extendibility and limitations as described earlier for laser melt annealing. Table 4c shows the values for SPE while achieving the 35nm node dopant activation target of 2.5E20/$cm^3$.

Earlier, the four requirements for shallow junction compatibility with high-*k* gate stack structures were listed in Table 1. The fourth item, "low junction leakage," refers to high quality SDE structures. This can easily be achieved on non-PAI wafers — but at the expense of $R_s$ — as reported by Tsuji, et al., and Kanemoto, et al., [32, 33]. On the other hand, with PAI techniques, they were able to achieve low $R_s$ but at the expense of degrading junction leakage. To improve junction leakage, both groups of researchers had to add an additional high-temperature RTA step similar to that reported earlier for laser melt annealing [26]. Tsuji's anneal at 900°C pushed the junction an additional 20.0nm. To overcome this, an experiment was designed (by the authors of this paper) to look at the relationship between dopant $X_j$ and PAI EOR depth ($X_j$–EOR, where EOR = end of range). Illustrated in Fig. 5 are the results for $R_s$ vs. junction leakage after SPE annealing for junctions with and without PAI.

Figure 6 illustrates how junction leakage can be reduced by confining the PAI EOR damage such that it remains in the junction ($X_j$–EOR>0), so that the electrical junction depth extends beyond the EOR damage created by the PAI region [34]. The $R_s$ values achieved with Si-PAI were about 15% lower than with Ge-PAI.

However, other investigators found that, by comparing Si and Ge PAI amorphous layer formation at the same depth and a 1E15/$cm^2$ dose, the amorphous interface with Ge was about 4× smoother compared to Si PAI [35]. When the junctions remained inside the Si-PAI material, junction leakage was in the 5E-3 to 2E-2A/$cm^2$ range (5–20pA/μm) and, as the junction extended beyond the Si-PAI, EOR damage junction leakage improved to 5E–5A/$cm^2$ (0.05pA/μm), as shown in Fig. 7. An example of this behavior is shown in Fig. 8, where SIMS profiles after SPE with various Si-PAI conditions at 1E15/$cm^2$ dose with plasma $BF_3$ implant at 5kV/2E16$cm^2$. Profile A is for no-PAI (no EOR), $X_j$ = 90.9nm, abrupt-

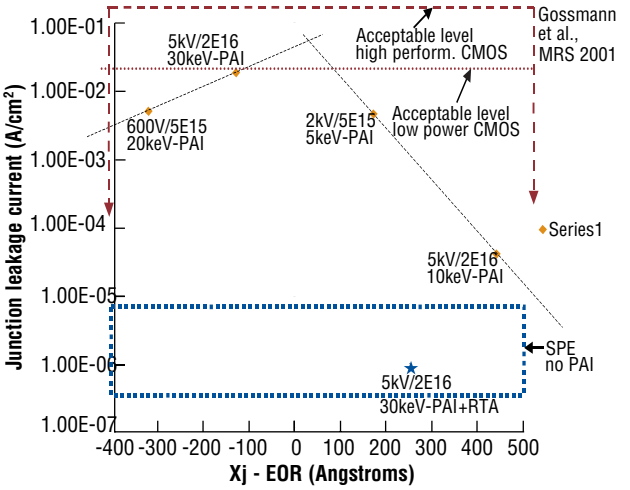


**Figure 7.** SPE junction leakage results for $X_j$ and PAI-EOR optimization.

ness = 22nm/dec, $R_s$ = 865Ω/sq., and leakage = 6.8E-6A/cm$^2$. Profile B is for 10keV Si-PAI (EOR = 23nm), $X_j$ = 67.1nm, abruptness = 16nm/dec, $R_s$ = 431Ω/sq. and leakage = 4.2E-5A/cm$^2$. Profile C is for 30keV Si-PAI (EOR = 60nm), $X_j$ = 46.9nm, abruptness = 10.9nm/dec, $R_s$ = 199Ω/sq. and leakage = 1.9E-2A/cm$^2$. Profile D is for 30keV Si-PAI (EOR = 60nm) and an additional 900°C/30 sec. RTA, with $X_j$ = 85.1nm, $R_s$ = 317Ω/sq. and leakage = 9.8E-7A/cm$^2$.

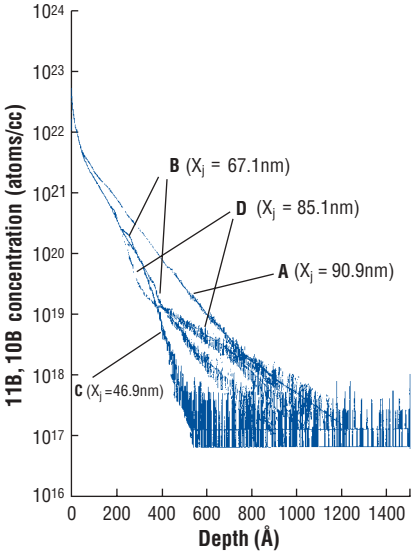


**Figure 8.** SIMS depth profile after SPE for plasma implanted $BF_3$ at 5kV/2E16/cm$^2$.

Through further optimization of the PAI process, such as using Ar, Ge, Sb, In,or other species to improve the amorphous interface roughness, it is believed that further reduction in leakage can be realized. However, the current level of junction leakage with SPE is within the acceptable range for high performance and low power CMOS. The off-current target values from the 2001 roadmap are listed in Table 5.

There are some companies developing the disposable spacer process for the 100nm technology node; low-temperature SPE formation of the SDE structure is an option being considered for implementation [10].

**Table 5 2001 ITRS off-current leakage targets**

| Node | 100nm | 70nm | 50nm |
|---|---|---|---|
| Year | 2003 | 2006 | 2010 |
| $X_j$ (nm) | 19–31 | 12–19 | 7–12 |
| $R_s$ | 550 | 830 | 830 |
| Dopant level/cm$^3$ | 8.00E+19 | 8.00E+19 | 1.50E+20 |
| **Leakage levels** | | | |
| Logic (pA/μm) | | | |
| High performance | 70 | 700 | 3000 |
| Low operating power | 100 | 300 | 1000 |
| Low standby power | 1 | 1 | 3 |

## Summary

With $SiO_2$ gate stack structures, high-temperature or low-temperature annealing techniques can be used with ion implantation for shallow junction formation satisfying the 50nm technology node requirements. With the planned insertion of high-*k* gates with metal electrodes starting at the 70nm node in 2006, new, low-temperature shallow junction processing will be needed. Using various PAI techniques, shallow and abrupt junctions (<8.0nm and <2.0nm/dec) with low $R_s$ (2.5E20/cm$^3$) and acceptable quality junction leakage (0.05pA/μm) have been achieved with 600°C SPE annealing. The low-temperature process integration constraints imposed with high-*k* gate low power CMOS makes SPE processing very attractive and the leading candidate for USJ formation. ■

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