Low Temperature Activation Of Ion Implanted Dopants: A Review
(Invited Paper)

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Abstract

Ion implanted dopants can be electrically activated through low temperature annealing in the 450°C to 800°C as reported in literature over the past 25 years. However, researchers in the last few years have applied this technique to realize ultra shallow junctions (USJ) for source drain extensions to satisfy the device junction roadmap requirements for the 65nm node and beyond. Therefore this paper will review the current status of low temperature annealing for USJ formation.

1. Introduction

According to the 2001 ITRS roadmap [1], maximizing device speed is critical for high performance logic for desktop computers and they will need very thin oxy-nitride gate dielectrics and low source drain parasitic resistance. Low leakage drives low power logic for portable/mobile systems like notebook computers and cell phones and they will need high-k gate dielectric for low leakage and higher source drain parasitic resistance is acceptable. The 65nm node (Lg<35nm) source drain extension targets for junction depth (Xj) is 13.5nm, lateral abruptness is 2.8nm/decade and Rs is 830 ohms/square. This means for example boron implant energies of 500eV with no dopant diffusion or 200eV with 5.0nm of diffusion. The implementation of high-k gate dielectrics will limit post gate formation processing temperatures to <700°C to prevent HfO dielectric material recrystallization [2]. Therefore the future need for low temperature process integration schemes is driving the recent renewed interest in low temperature USJ formation by solid phase epitaxy (SPE).

2. Low Temperature Activation

A. Historical Background

Back in 1977, Csepregi et al., reported on the recrystallization of silicon amorphous layers implanted with P, As and B ions in the 400-600°C range by SPE [3]. Soon after, Tsai & Streetman also reported on boron dopant activation in the 400-500°C for BF_2 and Si+B co-dopant implants [4]. Then 10 years later, Onishi et al. reported on a unique application of using low temperature boron SPE to characterize annealing equipment for temperature non-uniformities [5]. This is shown in Fig. 1 for boron implantation into crystalline silicon versus an amorphous silicon layer formed by Si implantation (Si-PAI) followed by furnace annealing in the 400-650°C range for 30 minutes. Over an order of magnitude lower Rs could be achieved with low temperature annealing with Si-PAI due to SPE. They calculated activation energies (1.9eV) as shown in Fig. 2 from the arrhenius plot and determined dopant activation levels (100ohms/square) from annealing times shown in Fig. 3. This allowed them to measure directly on each wafer temperature gradients before complete SPE recrystallization occurred and compare furnace to RTA annealing uniformities.

Expanding on this approach, Borland & Galewski reported on implanting dopants of B, Sb and P up to 1E16/cm2 doses directly into crystalline silicon for self amorphizing followed by low temperature SPE in the 420-550°C range on the heated chucks in various CVD systems from 3 to 30 minutes [6]. This allowed them to determine the actual wafer temperature and the wafer heating response for optimizing CVD chamber heater chuck designs. The phosphorus arrhenius plot is shown in Fig. 4. From the annealing time plot at 550°C shown in Fig. 5 dopant activation and complete SPE occurred between 3 and 5 minutes but the best Rs uniformity required SPE annealing up to 7 minutes (see Fig. 6). Another interesting phenomena reported by Mizushima et al., was the observed self-annealing of high dose boron implants in the mid E16 to E17/cm2 range [7]. In their paper they observed dopant activation not only in the 300-600°C range but also all the way down to room temperature.

B. Application to USJ

In their 1996 paper, Osburn et al. clearly illustrated the reduction in boron dopant diffusion

by lowering the annealing temperature from 1050°C down to 750°C as shown in Fig. 7 for boron plasma doping implantation [8]. Then in 1999, Tsuji et al. fabricated 50nm gate length pMOS devices using low temperature SPE at 550°C [9]. Their devices showed improved Vt roll-off but the end-of-range (EOR) damage left by the Ge-PAI layer degraded device leakage requiring an additional RTA 900°C 10 second anneal to further reduce the EOR defects and also drive the electrical junction beyond it. The improved leakage and Vt roll-off graphs are shown in Figs. 8 & 9.

The following year Kanemoto et al. also reported on SPE p+/n USJ formation using plasma implantation at 500V [10]. Their junction leakage results is shown in Fig. 10. Note that the SPE leakage result for the Si-PAI sample annealed at 850°C was the same as the non-PAI samples suggesting the junction had now diffused beyond the EOR damage caused by the 25keV Si-PAI (55.0nm). This lead to the work pursued by Borland et al. and Felch et al. [11,12 & 13] in trying to determine the optimized location of the EOR damage within the junction to achieve acceptable leakage of <2E-1 A/cm^2 for high performance CMOS and <2E-2 A/cm^2 for low power CMOS [14]. Their leakage results is shown in Fig. 11. Other interesting publications and presentations on low temperature SPE include Lindfors et al.[15 & 16], Lindsay et al. [17], Mansoori et al. [18] and Paton [19]. Mansoori showed how the SPE annealing could be incorporated into the side wall spacer formation step making this especially attractive when using a disposable spacer process flow. Figure 12 shows Rs versus Xj SPE results reported around the world and the limitation in boron dopant activation of 2.5E20/cm^3 [12].

C. Future Development

Besides further SPE process optimization to improve junction leakage, new ion implant equipment schemes are also being invented for low temperature dopant activation. Thakur et al. described the invention of a combined plasma ion implanter with an RTA heater for simultaneous implantation and annealing [20]. Dawson et al. on the other hand described a beamline implanter with a heated wafer holder also for simultaneous implant and annealing [21]. These approaches would require a thermal resistive mask such as a hard mask to be implemented.

3. Summary

In summary, ion implanted dopants can be electrically activated by low temperature SPE in the 450-750°C range resulting in shallow junctions of <13.5nm satisfying the 65nm node and beyond. To increase dopant activation Si or Ge-PAI are used to achieve 2.5E20/cm^3 boron electrically active levels. Additional research to improve junction leakage still needs to be done.

4. Acknowledgements

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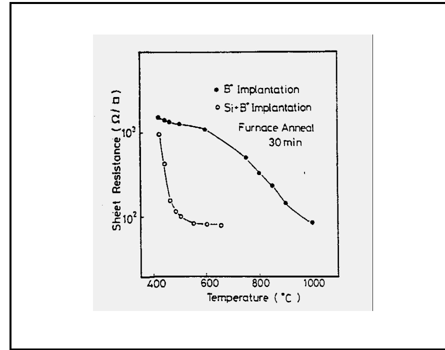

Fig. 1: Rs dependence on annealing temperature [5].

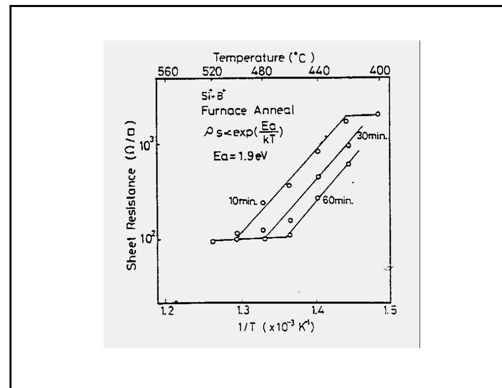

Fig. 2: Arrhenius plot for boron Rs versus 1/temp. [5].

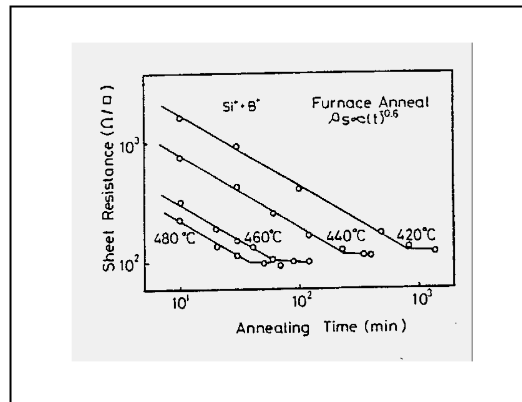

Fig. 3: Boron Rs versus annealing time [5].

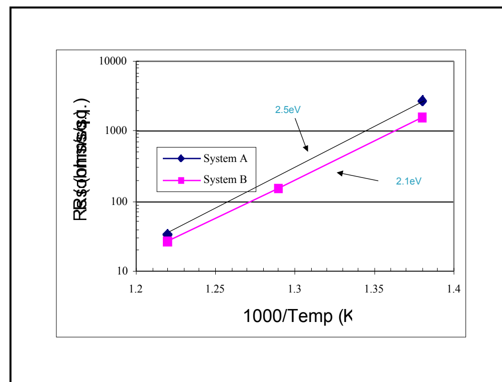

Fig. 4: Phosphorus Rs arrhenius plot [6].

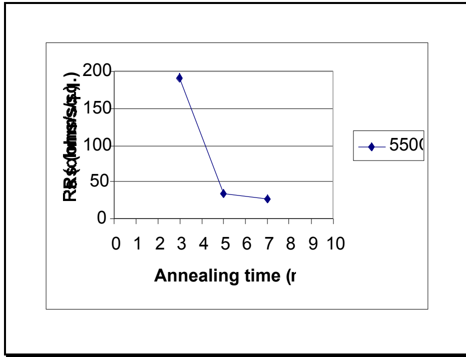

Fig. 5: Phosphorus Rs versus annealing time [6].

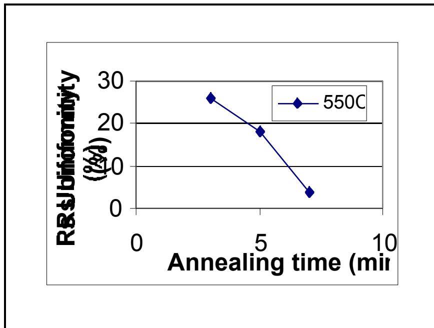

Fig. 6: Phosphorus Rs uniformity versus time [6].

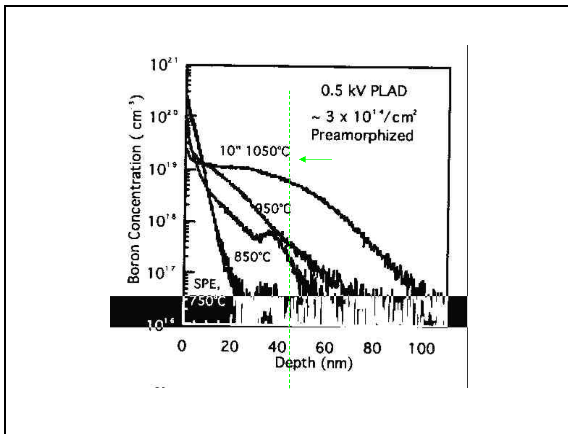

Fig. 7: Boron SIMS dopant profile [8].

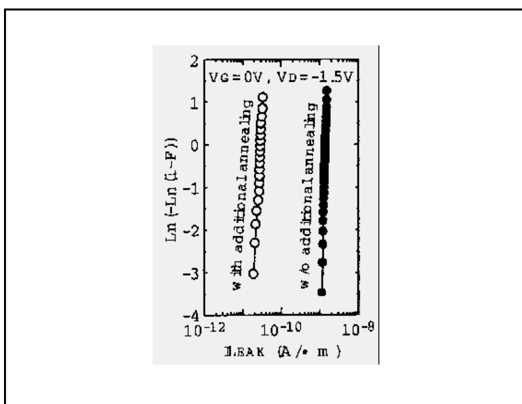

Fig. 8: Improved GIDL distribution with RTA [9].

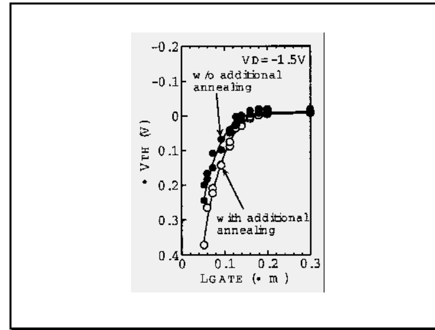

Fig. 9: Vt roll-off with additional RTA anneal [9].

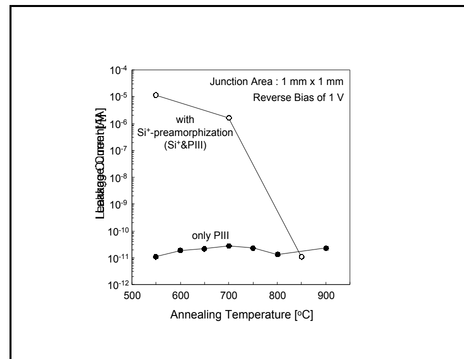

Fig. 10: Leakage current versus SPE annealing temperature [10].

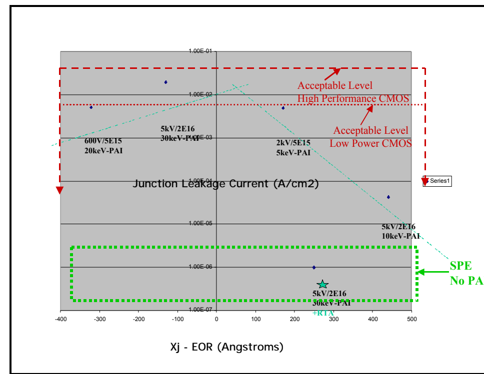

Fig. 11: Leakage current versus Xj-EOR for SPE [12].

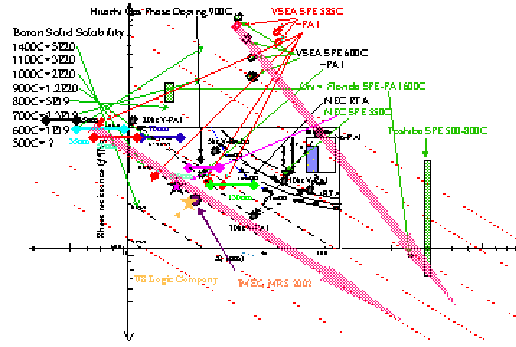

Fig. 12: Summary of Rs versus Xj SPE results [12].