Optimized BF_3 P^2LAD Implantation With Si-PAI For Shallow, Abrupt and High Quality p^+/n Junctions Formed Using Low Temperature SPE Annealing

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***Abstract*- Shallow junction formation by low temperature SPE (solid phase epitaxial growth) is an attractive activation technique, as it can be easily integrated into disposable spacer or high-k gate process schemes for sub-100nm technology nodes. In this paper we report our experimental results using BF_3 P^2LAD implantation at wafer biases between 600V and 5kV and low temperature SPE annealing in the 550-650ºC range to achieve shallow and abrupt p^+/n junctions. Using various Si-PAI (pre-amorphizing implantation) conditions between 5keV and 30keV, we were able to optimize the location of the PAI residual implant damage relative to the electrical junction depth to achieve acceptable junction leakage values. Using specially prepared samples with simulated pMOS dopant profiles, p^+/n junction leakage current as a function of the difference between the junction depth and the location of the PAI damage (X_j – EOR) could be determined. The X_j - EOR values were also verified by SIMS and cross-sectional X-TEM micrographs.**

I. Introduction

As technology advances and semiconductor devices continually shrink, the source/drain extension junction depths must decrease to minimize short-channel effects and maximize device performance. The 2001 version of the International Technology Roadmap for Semiconductors [1] predicts that the 70 nm technology node will require source/drain extensions with junction depths of 12-19 nm and a maximum sheet resistance of 830 ohms/sq. In addition, the gate dielectric equivalent oxide thickness must decrease, which necessitates the migration from SiO_2 to oxynitrides to high-k dielectrics. However, high-k dielectric materials cannot survive the high-temperature activation anneals that have been traditionally used, since these materials crystallize at such high temperatures. As a result, a low-temperature, alternative, annealing and dopant activation technique is needed. Solid phase epitaxy (SPE), where annealing occurs at temperatures of 550-700ºC, is one candidate to meet these needs [2,3,4,5]. This paper presents results of SPE annealing where the dopants were implanted by an alternative, ultra-low energy doping technology called Pulsed Plasma Doping (P^2LAD).

II. Experimental

All of the wafers used in this study were 200-mm, n-type, (100) silicon substrates with resistivities of 10-20 Ω-cm. The wafers were implanted without any pre-cleans. Some of the samples were pre-amorphized with Si^+ or Ge^+ ions, while the others remained as crystalline silicon. The dopant boron atoms were implanted with BF_3 Pulsed Plasma Doping using VSEA's P^2LAD research test stand [6]. Wafer biases of –600 V to –5 kV and targeted doses of 1-5 x 10^{15} cm^{-2} were studied. The SPE annealing was performed on a proprietary hot chuck at temperatures of 560-650ºC and times of 3-30 min. in a 1 x 10^{-6} Torr vacuum.

Characterization of these samples consisted of sheet resistance measurements, Hall van der Pauw measurements, secondary ion mass spectrometry (SIMS) profiling, transmission electron microscopy (TEM), and reverse-bias diode leakage currents. The sheet resistance was measured at the center of a wafer with a manual, four-point probe, while the contact voltage was also measured to insure good pin contact to the doped region as opposed to punchthrough to the silicon substrate. The SIMS profiles were performed with a PHI quadrupole SIMS instrument using 1 keV O_2^+ primary ions at a 60º angle of incidence and oxygen leak. Both plan-view and cross-sectional TEM were used to measure the defect density after SPE and the location of any residual defects, respectively.

The quality of the p^+-n junctions formed with SPE annealing was evaluated with diode test structures. An n-well similar to that seen in actual pMOS devices, with an average dopant concentration of about 5 x 10^{17} cm^{-3}, was first formed by a series of 4 implants (500 keV P^+ at 2 x 10^{13} cm^{-2}, 250 keV P^+ at 1 x 10^{13} cm^{-2}, 100 keV P^+ at 5 x 10^{12} cm^{-2}, and 20 keV P^+ at 1.2 x 10^{12} cm^{-2}) followed by a furnace anneal at 800ºC for 30 min. in O_2. Most of the diode wafers were then pre-amorphized with Si^+ ions with energies of 5-30 keV to a dose of 1 x 10^{15} cm^{-2}. Next, the boron dopant was introduced with BF_3 P^2LAD at wafer biases of –0.6 kV to –5.0 kV and targeted doses of 5 x 10^{15} cm^{-2} or 2 x 10^{16} cm^{-2}. An SPE anneal at 560ºC for 15 min. followed the P^2LAD step. Finally, mesa

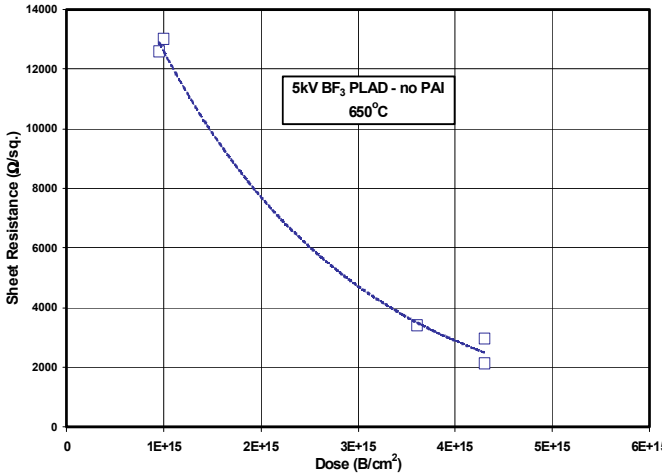

Figure 1. Sheet resistance as a function of P^{2}LAD dose for non-preamorphized samples.

diode structures were formed by application of Apiezon wax dots, wet etch of the exposed silicon, and removal of the wax. The reverse bias leakage current density was measured at –1 V with a 3-probe method: two probes on the implanted electrode for bias supply and bias voltage measurement and one probe on the silicon base for collecting the leakage current.

III. Results and Discussion

Sheet resistance as a function of P^{2}LAD dose for non-preamorphized samples is presented in Fig. 1. The boron ions were implanted with 5.0 kV P^{2}LAD, followed by a 650ºC SPE anneal. The most striking observation from this data is the extremely high sheet resistance values. Clearly this anneal with non-preamorphized substrates does not produce junctions that satisfy the sheet resistance requirements of advanced devices. Nevertheless, these wafers do exhibit decreasing sheet resistance with increasing dose, as is traditionally observed with high-temperature anneals.

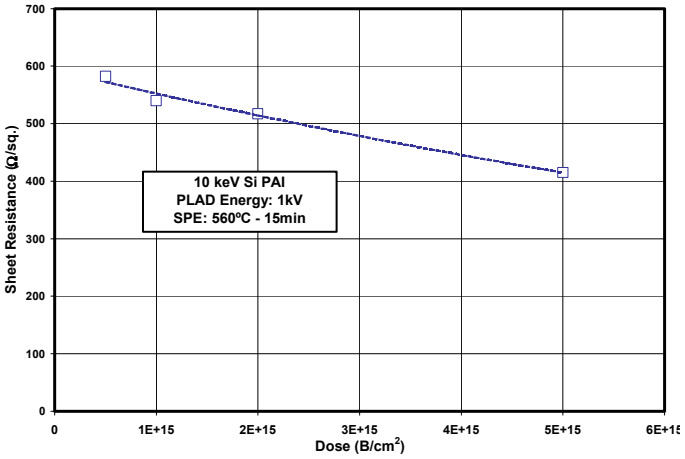

Figure 2. Sheet resistance as a function of P^{2}LAD dose for samples pre-amorphized with 10 keV Si^+ ions to a dose of 1 x 10^{15} cm^{-2} and annealed at 560ºC for 15 min.

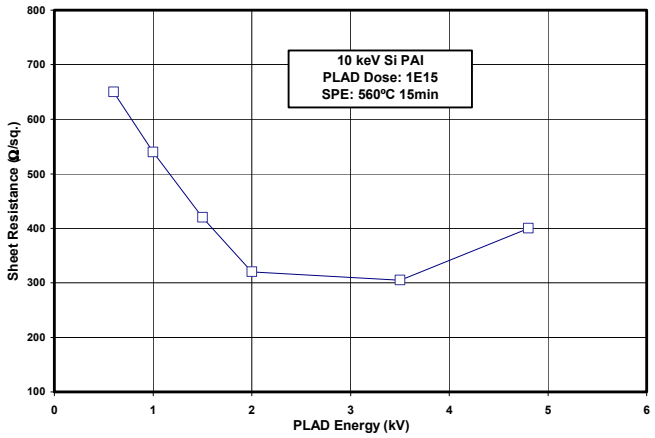

Figure 3. Sheet resistance as a function of P^{2}LAD energy for samples pre-amorphized with 10 keV Si^+ ions to a dose of 1 x 10^{15} cm^{-2} and annealed at 560ºC for 15 min.

Fig. 2 displays the sheet resistance as a function of P^{2}LAD dose for samples pre-amorphized with 10 keV Si^+ ions to a dose of 1 x 10^{15} cm^{-2} and annealed at 560ºC for 15 min. For the P^{2}LAD wafer bias of 1 kV, all of the dopant is located in amorphous silicon. As a result, the expected trend of lower sheet resistance with increasing dose is observed.

Sheet resistance as a function of P^{2}LAD energy for samples pre-amorphized with 10 keV Si^+ ions to a dose of 1 x 10^{15} cm^{-2} and annealed at 560ºC for 15 min. is shown in Fig. 3. As the PLAD wafer bias is increased from 0.6 kV to 2 kV, the sheet resistance decreases due to the larger number of dopants under the solid solubility limit, which can be electrically activated. However, when the wafer bias is increased to 5 kV, a substantial amount of the dopant lies in crystalline silicon beyond the amorphous/crystalline interface and thus is not activated by the SPE anneal, resulting in an increased sheet resistance.

Fig. 4 exhibits depth profiles of boron concentration measured by SIMS for wafers pre-amorphized with 30 keV Ge^+ ions to a dose of 1 x 10^{15} cm^{-2}, plasma-doped with boron

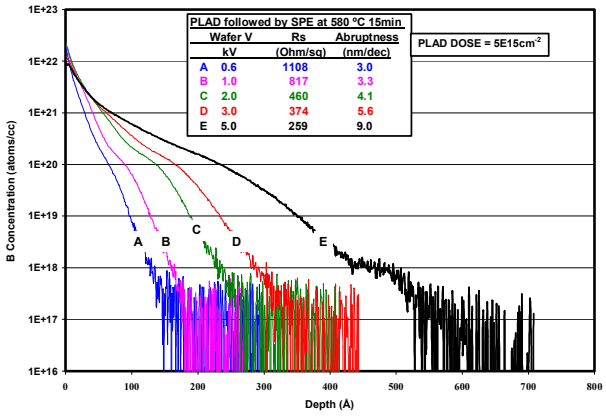

Figure 4. Depth profiles of boron concentration measured by SIMS for wafers pre-amorphized with 30 keV Ge^+ ions to a dose of 1 x 10^{15} cm^{-2}, plasma-doped with boron to a dose of 5 x 10^{15} cm^{-2}, and SPE-annealed at 580ºC for 15 minutes.

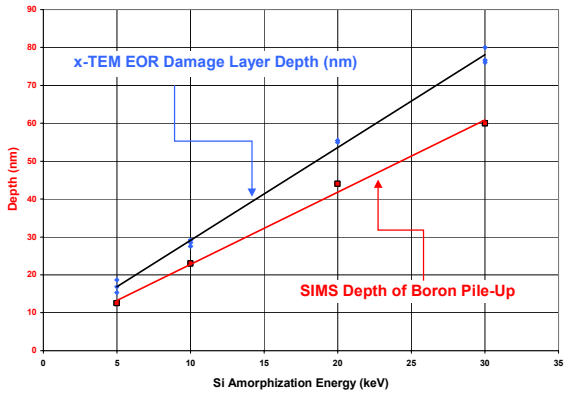

Figure 5. Boron pile-up depth as measured by SIMS and EOR damage layer depth as measured by cross-sectional TEM for various Si^+ pre-amorphization energies.

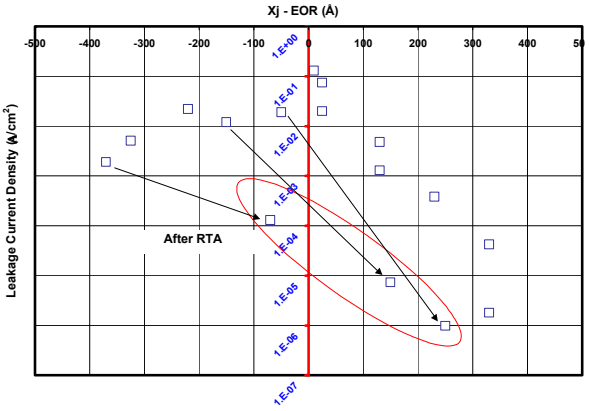

Figure 7. Leakage current density for p^+-n diodes as a function of the difference between the dopant junction depth and the location of pre-amorphization end-of-range defects (X_j – EOR).

to a dose of 5 x 10^{15} cm^{-2}, and SPE-annealed at 580ºC for 15 minutes. The profiles for 5 different P^2LAD wafer biases show that the profiles continually become deeper as the wafer bias increases. All of the profiles closely resemble their respective as-implanted profiles, except for the 5.0 kV profile which has some dopant pile-up between 43 and 50 nm. Since the amorphous layer thickness for this pre-amorphization condition can be estimated to be about 40-45 nm [7,8], the defects associated with the amorphous/crystalline interface (often called end-of-range [EOR] defects) must be responsible for gettering some boron to that region. Cross-sectional TEM measurements were made to confirm that the damage layer depth agreed with the pile-up depth measured by SIMS (see Fig. 5). The pile-up depths were found to be about 28% shallower, which could possibly be explained by differences in the two techniques' depth calibrations or if the dopants actually segregate to a region just before the damage layer.

A plot of sheet resistance as a function of junction depth for several samples that were pre-amorphized with Si^+ or Ge^+ ions and annealed by SPE is presented in Fig 6. The requirements of the various technology nodes as predicted by the 2001 ITRS [1] are also included. The dashed line

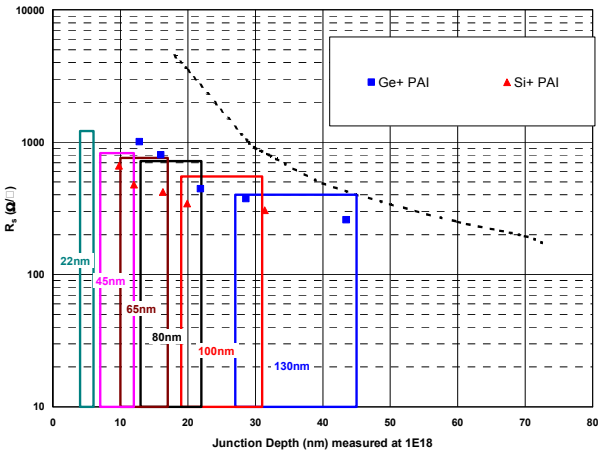

Figure 6. Sheet resistance as a function of junction depth for several samples that were pre-amorphized with Si^+ or Ge^+ ions and annealed by SPE.

represents the "SEMATECH" curve, which indicates the lower limit attained by a collection of rapidly annealed, B^+-implanted wafers. These data show that the sheet resistance values obtained with Si^+ PAI are substantially lower than those obtained with Ge^+ PAI, especially for the shallowest junction depths. More importantly, SPE on Ge^+ PAI wafers appears to satisfy the requirements of the 80 nm technology node and just touches the 65 nm node, while SPE on Si^+ PAI wafers seems to reach the 45 nm node.

Fig. 7 displays the leakage current density for p^+-n diodes as a function of the difference between the dopant junction depth and the location of pre-amorphization end-of-range defects (X_j – EOR). When the junction depth is close to the EOR region, the residual defects lie in the junction's depletion region and contribute to high leakage current values, as observed. As the junction depth moves away from the EOR region in either direction, fewer defects are located in the depletion region and the leakage current improves. In particular, when a PAI energy of 10 keV and a P^2LAD condition of 5 kV and 2 x 10^{16} cm^{-2} were used, leakage current densities of 4.2 x 10^{-5} and 1.8 x 10^{-6} A/cm^2 were obtained, which are significantly below the ITRS acceptable level for off-state leakage of low-power CMOS devices [1,9]. In addition, when the diodes were subsequently annealed at 900°C for 30 s, the leakage current density was reduced by several orders of magnitude as many of the defects were annealed out and/or the junction depth moved even further from the EOR region.

The leakage current densities for diodes that had not been pre-amorphized were very low (between 4 x 10^{-7} and 7 x 10^{-6} A/cm^2). However, the sheet resistances of these junctions were extremely high, making them unacceptable for use in actual devices.

Defect density as measured by plan-view TEM is relatively constant regardless of the PAI or P^2LAD process conditions and varies between 4.5 x 10^{10} and 1.5 x 10^{11} defects/cm^2. However, large variations in the leakage current were observed as the separation between the junction depth and PAI end-of-range defects changed, as discussed above. This suggests that good junctions can be formed by SPE as long as the junction

depth and EOR are sufficiently separated, even though defects might still be present within the doped region. In order to satisfy the simultaneous requirement for ultra-shallow and low-leakage junctions, the PAI energy must be very low so that a reasonable P^2LAD bias can be used, or a very high PAI energy must be used so the amorphized region is much deeper than the doped region.

CONCLUSION

An assessment of SPE annealing with Si^+ and Ge^+ pre-amorphization and BF_3 Pulsed Plasma Doping was conducted. The sheet resistance was found to decrease with increasing dose and with increasing P^2LAD wafer bias as long as the dopant lies within the amorphized region. In addition, acceptable diode leakage current densities were measured when the junction depth is sufficiently displaced from the EOR region. Finally, SPE with Si^+ pre-amorphization appears to satisfy the requirements of the 45 nm technology node, suggesting that SPE is a promising, low-temperature activation technology for the future.

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