Low Temperature Shallow Junction Formation For 70nm Technology Node And Beyond

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ABSTRACT

Low temperature shallow junction formation is an attractive activation technique for 70nm technology node and beyond as it can easily be integrated into device structures that are formed using disposable spacer (reverse source drain extension formation) or low power CMOS devices using high-k/metal gate stack structures. Therefore, this paper will first review the shallow junction requirements as stated in the 2001 ITRS (international technology roadmap for semiconductors) and it's interpretation to ion implantation shallow junction formation for various dopant activation and annealing techniques. First high temperature (>1000^{o}C) RTA spike, flash or sub-melt laser annealing techniques with oxide or oxynitride/polysilicon electrode gate stack structures will be discussed and its limitations to <8E19/cm^{3} boron electrically active dopant level due to boron solid solubility limit in silicon satisfying only the 100nm technology node requirement (2003). Next, higher temperature laser melt annealing (1200^{o}C to 1400^{o}C) will be discussed and it's applicability beyond 70nm node technology (2006) to 25nm node (2016) where boron solid solubility limit is up to 5E20/cm^{3}. However, if high-k (HfO) dielectric/metal electrode gate stack structures are to be used starting at sub-100nm node in 2005 for low power CMOS then low temperature (<700^{o}C) annealing must be used for shallow junction formation to prevent recrystallization and dielectric constant degradation. Using low temperature SPE (solid phase epitaxial regrowth) annealing techniques in the 550^{o}C to 750^{o}C for short anneal times of <5mins., shallow & abrupt junctions 8.0nm deep, <2.0nm/decade with up to 2.5E20/cm^{3} boron electrical active dopant level can be achieved satisfying the 25nm technology node (2016) requirements.

INTRODUCTION

With the continued growth trends in portable/mobile devices replacing stationary desk top devices, more and more emphasis is being placed on improving low power CMOS devices. This is driving the switch from oxynitride type gate dielectrics with polysilicon electrodes to high-k (HfO_2) dielectrics with metal electrodes by 2005 to satisfy the 70-90nm technology node. High-k dielectric material have demonstrated orders of magnitude reduction in gate leakage with super thin equivalent gate oxide thicknesses but their control and deposition process are still very immature and therefore the focus of development at consortiums such as International-SEMATECH and SELETE. However, a fundamental high-k dielectric and metal electrode material issue is it's thermal stability and thermal resistance properties at elevated (high) temperatures above 700^{o}C. Several groups have reported the thermal stability of amorphous high-k dielectric is limited to <700^{o}C for HfO_2 and <800^{o}C for ZrO_2 before recrystalization occurs degrading the dielectric constant [1]. Selection of the metal electrode material can also

impose thermal budget limitations. To avoid these thermal budget constraints in the formation of shallow junctions the replacement gate process scheme was proposed several years ago [2,3]. Unfortunately, the replacement gate process has proven to be very difficult to manufacture and abandoned by most. The replacement gate process adds 2+ masking levels and 20% more processing steps [2]. Another issue is the key-hole structure resulting from the metal electrode deposition process due to the narrow aspect ratio [3]. Others have reported the difficulty of pre-cleaning the silicon surface prior to high-k dielectric deposition and this becomes extremely more difficult in the replacement gate structure where you have the narrow and steep side-wall geometries of the removable dummy gate structure to deal with. Therefore, with the conventional gate stack formation scheme for high-k dielectric with metal electrodes, the ion implanted shallow junction formation process will require a paradigm shift from high temperature annealing (>1000^{o}C) to low temperature annealing (<700^{o}C) for dopant activation and defect location engineered annealing for both SDE (source drain extension) and deep source drain formation. For this reason most of all the advanced logic manufacturers around the world are now investigating low temperature SPE in detail, implanting amorphous shallow junction structures using beam-line B_{11} and BF_2 species or plasma BF_3 and B_2H_6 species with various PAI (pre-amorphizing implant) conditions in the temperature range of 550^{o}C to 700^{o}C. Some of these results will be discussed below describing how to achieve: 1)low temperature (<700^{o}C), 2)shallow & abrupt junctions, 3)low resistance and 4)high quality (acceptable leakage) SDE structure that satisfies the 70nm technology node and beyond.

2001 ITRS SHALLOW & ABRUPT JUNCTION ROADMAP

The 2001 ITRS SDE junction depth, sheet resistance and lateral abruptness is shown in table I [4]. However, another key SDE parameter that was not identified in the 2001 ITRS is the SDE under diffusion (gate overlap) value. Ghani et al from Intel reported in their paper on CMOS scaling, projections of transistor parameters including the critical SDE shallow junction for both vertical (X_j) and lateral (Y_j) dimensions[5]. The lateral Y_j coorelates to the amount of gate under diffusion of the SDE structure also know as gate overlap. They showed insufficient gate overlap can degrade I_{DSAT} however improving lateral junction abruptness from 7nm/decade down to 1.5nm/decade improves it. With 7nm/dec. abruptness their 180nm technology transistors needed >20nm gate overlap while with 3.5nm/dec. lateral abruptness they could reduce gate overlap by 12.5nm to >7.5nm. Similarly, Osburn et al also reported on lateral dopant abruptness and for extreme abruptness <1.0nm/dec. negative gate overlap (gate underlap) of 5.0nm is desirable as shown in figure 1 [6]. Reducing gate overlap improves SCE (short channel effects) not only for bulk CMOS but also for SOI-CMOS [7]. With the insertion point for high-k gate with metal electrodes in 2006 for the 70nm node low power CMOS devices and 2010 for the 50nm high performance MPU CMOS devices the USJ (ultra shallow junction) roadmap for dopant and activation methods based on gate stack structure is shown in figure 2 [8]. Note the emergence of high-k/metal gate stack structure option in 2006 with low temperature dopant activation methods and new plasma doping method. Also, by 2007 elevated source/drain structures will re-emerge for thin SOI applications and shallow source drain structures requiring low parasitic source drain resistance. The universal Rs-vs-Xj chart with technology node windows and boron dopant activation levels (solid solubility limits) for a box profile 1st created by Shishiguchi of NEC and modified by Osburn of NCSU, Muto of I-SEMATECH and Borland of VSEA is summarized in figure 3 [9-12]. From this chart, 70nm node requires box profile

boron dopant level of 1E20/cm^3, while 50nm node requires a level of 1.5E20/cm^3 and 35nm node requires a level of 2E20/cm^3. Note the dramatic change between the 1999 and 2001 ITRS roadmap for Rs (sheet resistance) values. This came about from the device simulation studies reported by Kim et al of UCLA and Gossmann et al of Agere where they showed that a more relaxed specification window in Rs is acceptable in the 750 to 2000 ohms/square range rather than 200 to 300 ohms/square range [13,14].

Table 1. 2001 ITRS [4].

Year of Production	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM 1/2 Pitch [nm]	130	115	100	90	80	70	65	45	32	22
MPU/ASIC 1/2 Pitch [nm]	150	130	107	90	80	70	65	50	35	25
MPU Printed Gate Length [nm]	90	75	65	53	45	40	35	25	18	13
MPU Physical Gate Length [nm]	65	53	45	37	32	28	25	18	13	9
Equivalent physical oxide thickness for MPU/ASIC Tox[nm]	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
Gate Electrode Thickness [nm]	65-130	53-106	45-90	37-74	32-64	30-60	25-50	18-36	13-26	37517
Profile Control (side wall angle)	>89	>89	>89	90	90	90	90	90	90	90
Drain Extension Xj [nm]	27-45	22-36	19-31	15-25	13-22	12-19	10-17	7-12	5-9	4-6
Maximum Drain Extension Rs (PMOS) [Ohm/Sq]	400	460	550	660	770	830	760	830	940	1210
Extension Lateral Abruptness [nm/decade]	7.2	5.8	5.0	4.1	3.5	3.1	2.8	2.0	1.4	1.0

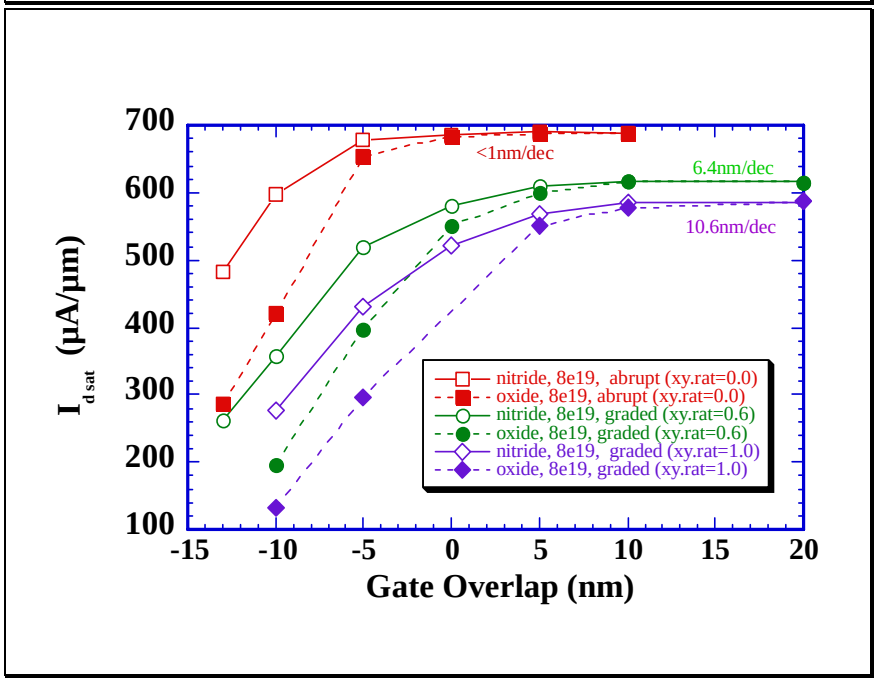

Figure 1. Lateral gradient (abruptness) effects on gate overlap requirements [6].

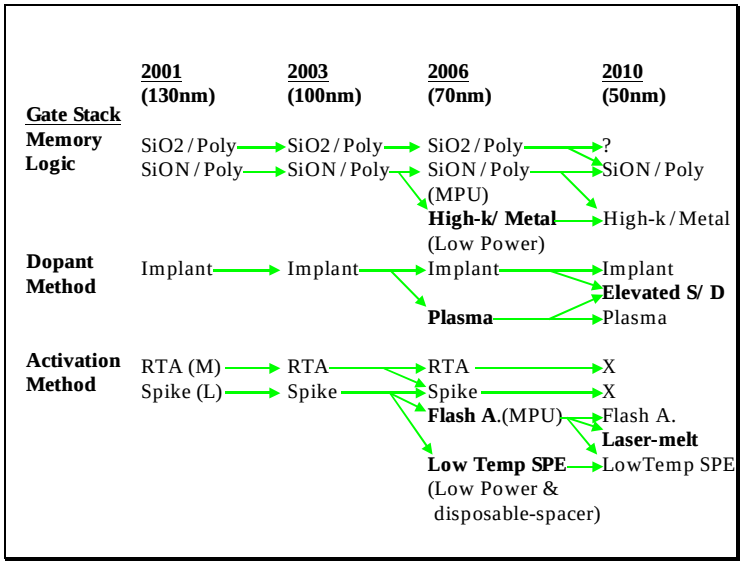

Figure 2. USJ dopant & activation roadmap [8].

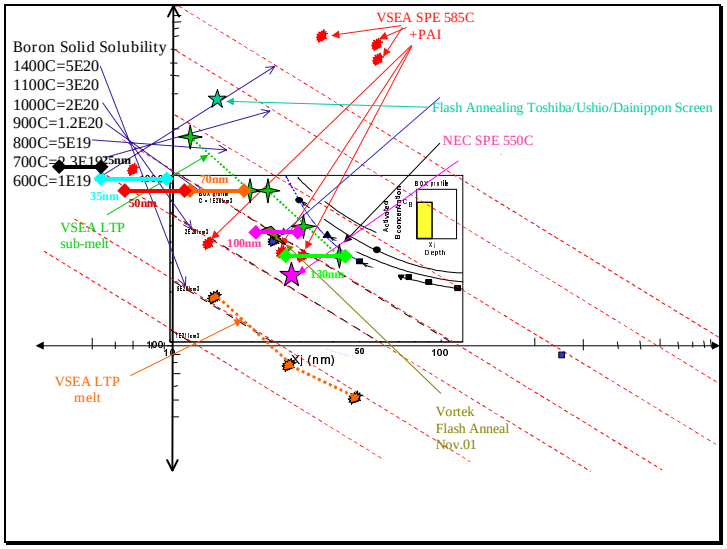

Figure 3. Rs-vs-Xj annealing results.

HIGH TEMPERATURE ANNEALING

RTA spike, flash and non-melt laser annealing

The most advanced annealing technique used in current state-of-the-art 130nm production manufacturing in 2002 is RTA spike annealing with controlled oxygen to reduce OED (oxidation enhanced diffusion) with beam-line implant energies down to 500eV in decel mode for B_{11} and 2keV for BF_2 requiring <0.3% energy contamination to achieve <22.0nm as-implanted Xj (junction depth) at 1E18/cm^3 and in drift mode <0.05% energy contamination to achieve 14.3nm as-implanted Xj and abruptness of 3.0nm/decade as shown in figure 4 [15]. Development for 100nm technology is being done at energies as low as 200eV in decel mode for B_{11} and 1keV for BF_2 with 0.3% energy contamination to achieve as-implanted X_j <18.0nm. For

70nm R&D development, drift mode implantation is required with no energy contamination (<0.05%) at 200eV B_{11} is being used to achieve 9.0nm as-implanted X_j value at 1E18/cm^3 level with 2.1nm/decade abruptness [16]. Using BF_2 higher implant energies are possible as well as better amorphization but there have been some reported concerns with F impurity affecting SiO_2 gate oxide quality [17]. However, use of BF_2 implantation can be extended through optimized oxynitride gate dielectric material [18]. Optimizing high temperature RTA annealing conditions can significantly impact junction depth (X_j). Shishiguchi et al showed the benefits of PAI on reducing TED (transient enhanced diffusion) for B_{11} implants >1keV [9]. Downey et al reported on the influence of controlled oxygen ambient during RTA processing to reduce OED (oxidation enhanced diffusion) [19]. Also, for sub-keV B_{11} implants, high ramp-up and cool-down rates both have been reported to reduce X_j while controlled oxygen showed minimal effects for sub-keV implants as reported by Matsuda et al [20]. However, sub-keV B_{11} implants using PAI of Si or Ge with RTA spike annealing produced deeper junctions than non-PAI. Sub-keV B_{11} implants also show surface dose sputtering limit as the energy is reduced below 500eV and the dose increases above 2E15/cm^2 as reported by Jacobson et al [21].

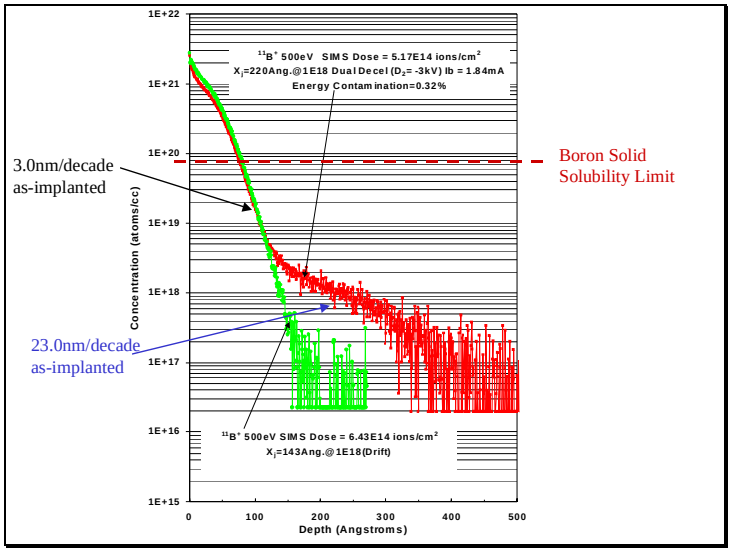

Figure 4. 500eV boron implant profile compare decel (0.3% energy contamination) to drift [15].

High temperature (1050C) RTA spike annealing on the average results in approximately 8.0nm of dopant diffusion from the as-implanted profile. Table 2 shows the direct interpretation of the ITRS roadmap in figure 1 in terms of junction depth Xj and Rs into implant energy and electrically active dopant concentration in silicon. Implant energies for both 0.3% and <0.05% energy contamination are shown for B_{11} and BF_2 spieces. Also, note that the limiter to this annealing methodology at 70nm node is implant energy for 0.3% energy contamination and fundamental dopant activation limit which seems to be at the solid solubility limit of boron in silicon, <8E19/cm^3 for a box like dopant profile corresponding to an equilibrium temperature of <900^{o}C as shown in figure 3. To further reduce dopant diffusion/movement and maintain the as-implanted profile with abrupt junctions super fast ramp-up and ramp-down rate annealing techniques have been proposed called flash annealing where the times are on the msec. (milli-second) duration. Examples include arc-lamp annealing, sub-melt laser annealing and most recently xenon lamp annealing [22,23,24]. Ito et al reported using standard tungsten halogen lamps on the bottom of an RTA system to heat the wafer first up to ~500^{o}C and then using xenon

top lamps to achieve flash annealing up to 1050°C in <30msec. Using a 200eV B_{11} implant they achieved X_j=15nm and Rs=3K ohms/sq. (3E19/cm^3)as shown in figure 3 and they stated this is their target for 70nm node devices which is 3.5x higher than the target Rs value stated in the 2001 ITRS [24]. Figure 3 also shows the results from Vortek's arc lamp flash annealing and Verdant's laser non-melt flash annealing techniques achieving Rs values equivalent to 1E20/cm^3 and 8E19/cm^3 respectively. Note that the best high temperature annealing result is only 1E20/cm^3 equivalent to 900°C solid solubility limit of boron in silicon. Therefore, the best high temperature flash annealing technique can satisfy only two out of the four requirements for high-k USJ process integration: 1) shallow & abrupt junctions and 2) high quality junctions and falls short on 3) low Rs and 4) low temperature annealing requirement of <700°C.

Table 2. 2001 ITRS interpretation for high temperature RTA spike anneal assuming 8.0nm diffusion in as-implanted X_j.

	130nm	100nm	70nm	50nm	35nm
Year	01	03	06	10	13
Xj	27-45nm	19-31nm	12-19nm	7-12nm	5-9nm
Xj-8nm	(19-37)	(11-23)	(4-11)	(-1-4)	(-3-1)
Rs	400	550	830	830	940
Dopant Level/ cm3	5E19	8E19	1E20	1.5E20	2E20
Dose Range	0.5-1E15	0.5-1E15	0.5-1E15	BSS	BSS
B11 (0.3% E. C.)	<1keV	<100eV	-	-	-
(No E. C.)	0.7-1.3keV	300-800eV	<300eV	-	-
BF2	1.9-4.8keV	0.2-2.2keV	<200eV	-	-
(no E.C.)	3.5-6.5keV	1.5-4.0keV	<1.5keV	-	-
PLAD	1.2-2.5kV	0.4-1.7kV	<400V	-	-

Laser melt annealing

High temperature laser annealing has been studied for over 25+ years and led to the development of RTA lamp annealing in the early 80's. Laser melt annealing in the 1200°C to 1400°C temperature range has been recently studied again for shallow junction formation. A key element to laser melt annealing is the location of the Ge-PAI layer which defines the melt region and therefore junction depth both vertically and laterally. The Ge-PAI layer is used to define the junction and lower the melting temperature of silicon by 200°C from 1400°C to 1200°C. Upon surface melting, the implanted boron dopant atoms rapidly and uniformly redistributes itself throughout the melted Si-Ge amorphous region at the boron solid solubility limit level at 1400°C (5E20/cm^3). However, one of the issues with this technique is the creation of EOR (end-of-range) damage that are present beyond the amorphous/crystalline interface leading to degradation in junction leakage current in both the vertical as well as in the lateral channel directions. To improve leakage the electrical junction must diffuse beyond the EOR damage as

reported by Talwar et al through an additional RTA anneal [25]. Using an additional 800°C 20 seconds RTA anneal after the laser melt annealing step they were able to drive the junction an additional 15.0nm deeper thus improving junction leakage however, this increased the junction depth by 33% from 45.0nm to 60.0nm and also resulted in dopant deactivation (solid solubility limit) effects. Takamura et al showed dopant deactivation in the 500°C to 900°C temperature range occurs within the first 10 sec. of an RTA anneal and can result in 30% to 75% dopant deactivation [25]. Nevertheless, table 3 summaries high temperature laser melt annealing results showing it's ability in achieving the high boron electrically active dopant level of 5E20/cm^3 for sub-25nm technology node but would require boron implant energies <100eV. As stated above, process integration and material compatibility are what will limit the production application of laser melt annealing. Also, post laser melt wafer thermal treatment resulting in dopant deactivation and solid solubility limit degradation in Rs value and the need to improve junction leakage by driving the junction deeper beyond the EOR defects which may negates all the advantages of laser melt annealing. The device level integration issues with laser melting must be overcome before this technique will be accepted in manufacturing and Talwar et al summarized their results with laser-melt annealing at the April 2001 Spring MRS meeting [26]. They include: 1) melting of the silicon under the STI (shallow trench isolation) structure which can result in the STI structure popping out, 2) polysilicon gate stack electrode melting and rounding and 3) optimization of lateral junction profile for gate over-lap and junction leakage control due to the lateral placement of the PAI layer.For high-k gate stack structures laser melting is not an option, therefore, limiting it's potential application to oxide or oxynitride /polysilicon gate stack structures only. For these reasons laser melt annealing has been abandoned by a number of leading logic device manufacturing companies and they have switched their attention to low temperature activation and annealing techniques since only two out of the four high-k gate stack integration shallow junction requirements can be achieved: 1) shallow & abrupt junctions and 2) low Rs and not meeting 3) the low temperature annealing requirement of <700°C and 4) the high quality junction based on low junction leakage current.

Table 3. 2001 ITRS interpretation for high temp. laser melt annealing (Xj=Ge-PAI EOR depth).

	130nm	100nm	70nm	50nm	35nm
Year	01	03	06	10	13
Xj	27-45nm	19-31nm	12-19nm	7-12nm	5-9nm
Rs	400	550	830	830	940
Dopant Level/ cm3	5E19	8E19	1E20	1.5E20	2E20
Dose Range	0.5-1E15	0.5-1E15	0.5-1E15	0.5-1E15	0.5-1E15
Ge-PAI	17-29keV	12-20keV	7-12keV	3-7keV	2-4.5keV
B11 (0.3% E. C.)	0.5-1.3keV	<500eV	-	-	-
(no E.C.)	1-1.7keV	0.6-1.1keV	300-600eV	150-300eV	80-200eV
BF2 (0.3% E.C.)	3-6.5keV	1.8-3.7keV	0.2-1.7keV	<200eV	-
(no E.C.)	5-8.3keV	3-5.5keV	1.5-3keV	0.75-1.5keV	0.4-1keV
PLAD	1.6-3kV	1.2-2keV	0.5-1.2kV	200-600V	100-300V

LOW TEMPERATURE ANNEALING (550°C TO 750°C) BY SPE TECHNIQUE

Low temperature SPE annealing has also been investigated over the last 25+ years but the need for a manufacturing solution when using high-k gate stack structures has created great interest in this technique over the last few year. With optimized SPE processing all four requirements for high-k USJ process integration can be realized: 1) low temperature <700°C annealing (600°C in 3.5 minutes), 2) shallow (8.0nm) & abrupt (<2.0nm/decade) junctions, 3) low Rs (2.5E20/cm^3) and 4) acceptable junction leakage (<20pA/um) for low power CMOS. The main focus on SPE research is optimizing acceptable level of junction quality through PAI optimization. Nevertheless, the top logic manufacturers in the US, Japan, Taiwan and Europe are all actively developing low temperature annealing processes for 70nm technology node driven by low power CMOS devices which will use high-k gate stack structures in order to reduce gate leakage [16]. At temperatures below 750°C dopant diffusion is not observed as reported by Osburn et al. comparing temperatures from 750°C up to 1000°C [27]. Using PAI of Si or Ge eliminates channeling thereby shallower junctions are realized with SPE techniques as shown in figure 5 for 600V and 2kV BF_3 plasma implantation, note this was not the case with high temperature RTA spike annealing as discussed earlier where PAI resulted in deeper junctions for sub-keV implants [9]. Also, abruptness of <2.0nm/dec. can be achieved as shown in figure 5 for 600V plasma implant. SPE recrystalization rates for various temperatures was reported by Jacobson where he observed the rate to be 0.1A/sec at 500°C, 1A/sec at 550°C, 10A/sec at 600°C, 100A/sec at 660°C, 1000A/sec at 730°C and 10,000A/sec at 830°C as shown in figure 6 [28]. Complete dopant activation by SPE at <600°C can be achieved in the 3 to 5 minute time frame for either PAI or non-PAI wafers as reported by Borland & Galewski [29]. Antimony SPE results were also reported by Ponmanev et al showing similar supersaturation levels to boron [30]. Figure 3 shows the low temperature SPE results from various organizations around the world using low temperature SPE annealing techniques showing dopant activation limit at the supersaturation level of 2.5E20/cm^3. Table 4 shows the extendability of SPE to sub-25nm technology node but would require implantation energies for boron below 100eV range in order to realize 5.0nm junctions.

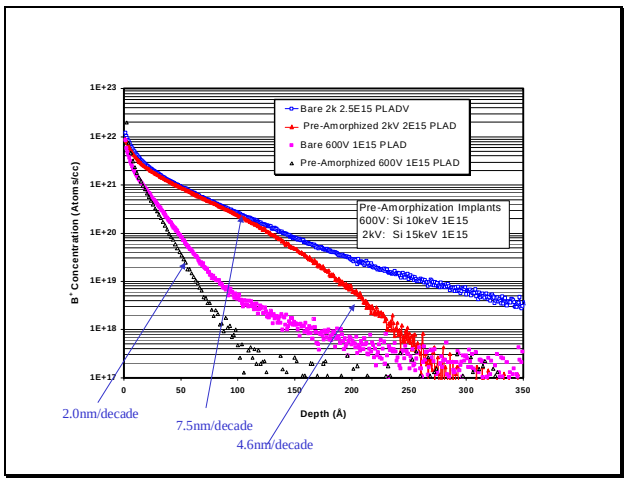

Figure 5. PAI for channeling reduction.

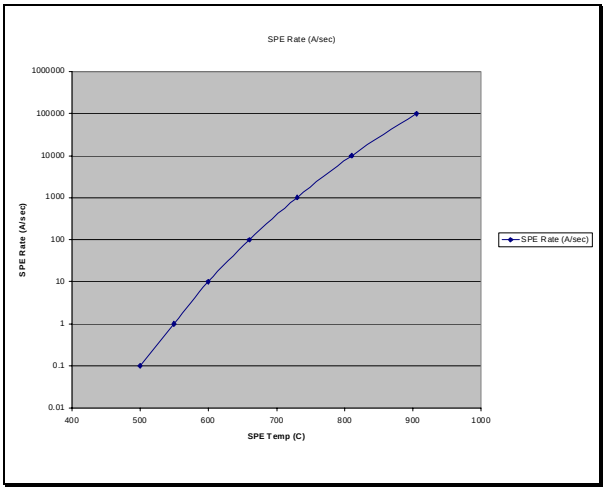

Figure 6. SPE recrystallization rate [28].

Table 4. 2001 ITRS interpretation for low temperature SPE (X_j=as-implanted junction depth).

	130nm	100nm	70nm	50nm	35nm
Year	01	03	06	10	13
Xj	27-45nm	19-31nm	12-19nm	7-12nm	5-9nm
Rs	400	550	830	830	940
Dopant Level/ cm3	5E19	8E19	1E20	1.5E20	2E20
Dose Range	0.5-1E15	0.5-1E15	0.5-1E15	0.5-1E15	5E15
Ge-PAI or	11-21keV	10-14keV	6-10keV	3-6keV	2.5-5keV
Si-PAI	9-16keV	7-10keV	4-7keV	2-4keV	2-3keV
B11 (0.3% E.C.)	0.5-1.3keV	<500eV	-	-	-
(no E.C.)	1-1.7keV	0.6-1.1keV	300-600eV	150-300eV	80-200eV
BF2 (0.3% E.C.)	3-6.5keV	1.8-3.7keV	0.2-1.7keV	<200eV	-
(no E.C.)	5-8.3keV	3-5.5keV	1.5-3keV	0.75-1.5keV	0.4-1keV
PLAD	1.6-3kV	1.2-2keV	0.5-1.2kV	200-600V	100-300V

Control of junction leakage is a major concern but on non-PAI wafers excellent junction leakage can be achieved with low temperature annealing below 600^{o}C but at the expense of Rs as reported by Tsuji et al and Kanemoto et al [31, 32]. With PAI techniques on the other hand, they were able to achieved low Rs but at the expense of degrading junction leakage. To improve junction leakage they both had to add an additional high temperature RTA step similar to that reported earlier by Talwar et al for laser melt annealing. Tsuji's anneal at 900^{o}C pushed the junction an additional 20.0nm. Therefore to overcome the need for the additional higher temperature anneal and dopant diffusion an experiment to look at the relationship between dopant Xj and PAI EOR depth (Xj-EOR) was conducted as illustrated in figure 7 [33]. Since SPE Rs values with Si-PAI was about 20% lower than with Ge-PAI, Si-PAI SPE wafers were used in the study. However, for a 1E15/cm^2 dose, the amorphous interface with Ge-PAI is about 4x smoother compared to Si-PAI [34]. Figure 8 shows results of Rs-vs-junction leakage for both non Si-PAI and Si-PAI wafers. Low Rs values were achieved with PAI. When the junctions remained inside the Si-PAI material, poor junction leakage resulted and as the junction extended beyond the Si-PAI EOR damage leakage improved as illustrated in figure 9. Through further optimization of the PAI process by using other implant species to improve the amorphous interface roughness it is believed further improvement in leakage can be realized. However, the current level of junction leakage with SPE is within the acceptable range for low power CMOS as reported by Gossmann et al and labeled in figure 9 for high performance CMOS at <20nA/um and low power CMOS at <20pA/um [14].

Some companies are developing the disposable spacer process for 100nm technology node and with this technique, low temperature SPE formation for the SDE structure is an option being considered for ease of process integration [16]. Alternatively, elevated S/D structures can also be integrated with low temperature SDE formation for improved salicide contacting.

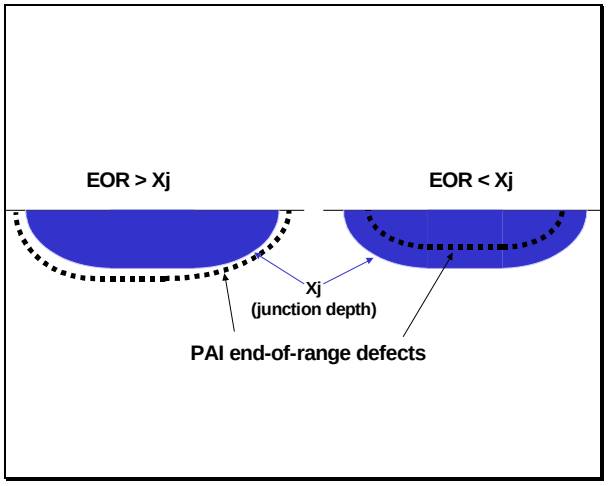

Figure 7. SPE leakage study for Xj-EOR sensitivity.

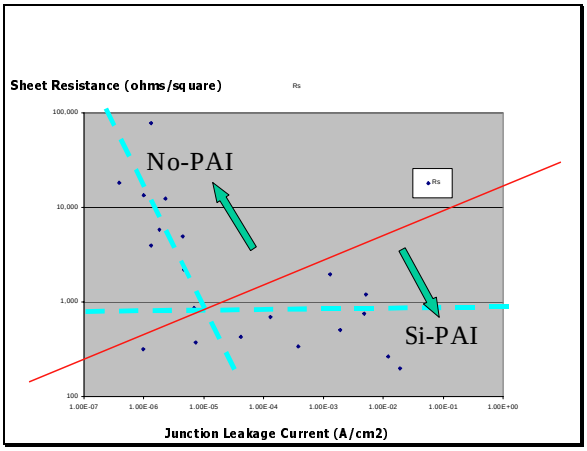

Figure 8. Influence of PAI on Rs-vs-junction leakage.

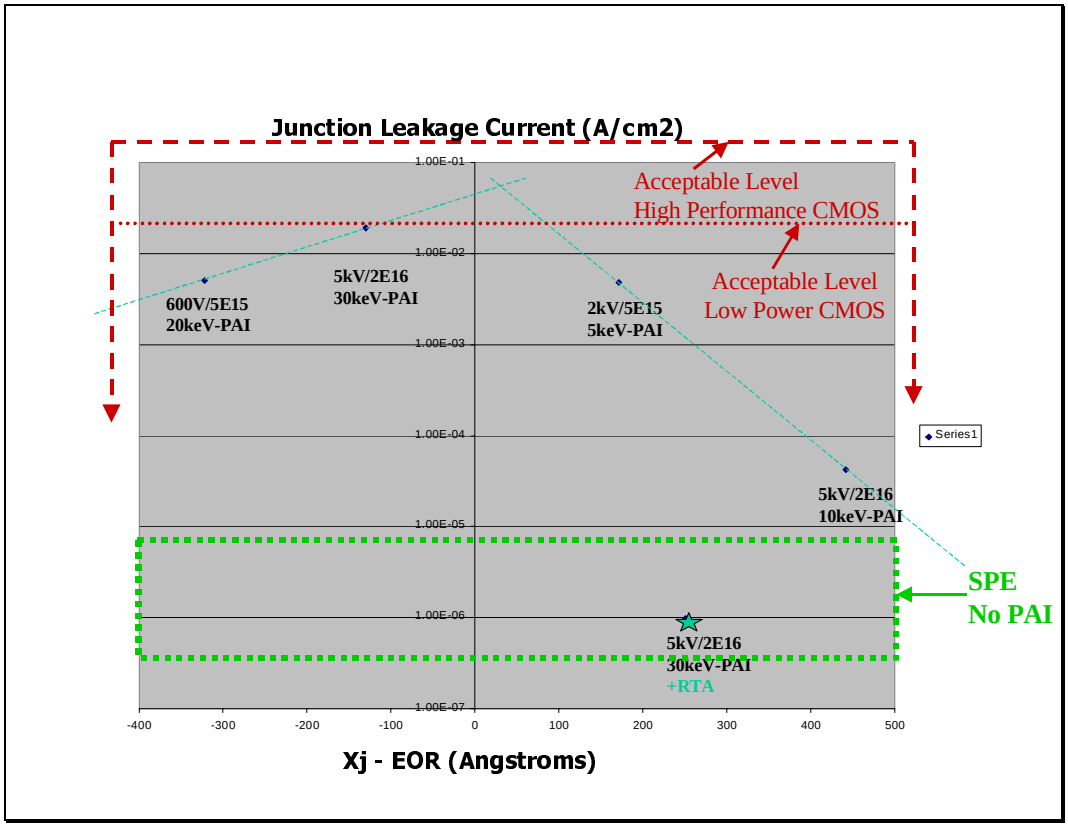

Figure 9. Sensitivity of Xj-EOR on junction leakage current.

SUMMARY

With oxide and oxynitride/polysilicon gate stack structures, high temperature (flash or laser melt) and low temperature annealing techniques can be used for implanted shallow junction formation in the conventional process flow or reverse flow disposable spacer technique for the

70nm technology node requirements and may be extended beyond with laser melt or SPE to 25nm node. With the planned insertion of high-k gates with metal electrodes for low power CMOS starting at 70nm technology node in 2006, new low temperature shallow junction processing techniques will be needed. Using various PAI techniques, shallow (8.0nm) & abrupt (<2.0nm/decade) junctions with low Rs (2.5E20/cm^3) and acceptable quality junction leakage (<20pA/um) have been achieved at 600°C satisfying the 2001 ITRS roadmap requirements for sub-25nm technology node but this would require boron implant energy below 100eV. The process integration constraints imposed with high-k gate stack structures requiring low temperature shallow junction formation makes SPE processing very attractive and the leading candidate for 70nm and beyond USJ formation for both classical and non-classical CMOS using bulk or SOI wafer technology.

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