IMPROVED DEVICE SCALING & PROCESS SIMPLIFICATION THROUGH ADVANCED ION IMPLANTATION TECHNIQUES

John O. Borland
Varian Semiconductor Equipment Associates
4 Stanley Tucker Dr.
Newburyport, MA 01950

ABSTRACT

Advanced ion implantation techniques are being used to solve device scaling issues through the use of equivalent scaling methodology. These include vertical device isolation and manufacture of SOI wafers by hydrogen or oxygen ion implantation, improved lateral device isolation through parallel beam high energy implantation, higher-k gate material modification through selected impurity implantation such as nitrogen into silicon dioxide, improved device Leff control through zero tilt shallow junction implantation and high tilt implantation for gate overlap control. Additional cost savings and 2 to 4 mask count reduction have been achieved through post-gate implant (PoGI) process simplification technique. Besides beam-line single wafer implanter designs, new cluster module designs are appearing using plasma doping techniques.

INTRODUCTION

With the problems associated with continued conventional device scaling and the move to SOC (system on a chip) with embedded memory and logic devices the industry is facing a new paradigm shift. Conventional scaling has been reported to be less effective for sub-130nm SOC technology so the industry is moving to equivalent scaling (1). Equivalent device scaling is achieved through; 1) new materials such as SOI wafers and higher-k gate materials, 2) new processes such as multiple gate oxides and shallow junction formation processes and 3) new device structures such as notched poly, FD/PD SOI, double gate and vertical transistors. Therefore, this paper will discuss how the use of advanced ion implantation techniques is solving equivalent scaling issues in the areas of: 1) wafer and isolation engineering for improved vertical and lateral device isolation, 2) gate material modification through ion implantation for multiple gate oxide thickness for embedded memory and logic technologies and to achieve higher-k gate dielectric to lower gate leakage, 3) channel and S/D engineering for shallow junction formation, gate overlap control and short channel effect (SCE) control, 4) process simplification and lithography mask count reduction and 5) new advanced ion implanter designs to achieve these results.

DEVICE VERTICAL & LATERAL ISOLATION

Both lateral and vertical device isolation improvements can be realized through advanced implantation techniques. 80 to 90% of SOI wafers are manufactured with either an oxygen or hydrogen implantation step for vertical isolation. SIMOX (Separation by IMplantation of OXygen) SOI wafers are manufactured by high dose (E17 to E18/cm2) oxygen implantation and was first reported 20 years ago by researchers from NTT. In this technique oxygen is implanted directly into the silicon wafer and a buried oxide layer is formed by a high temperature 1350°C 6 hour anneal/oxidation process (2). IBIS Technology, Nippon Steel and Komatsu Materials are examples of SIMOX SOI wafer manufacturers. The other SOI manufacturing method uses hydrogen implantation (E16/cm2) to form a splitting buried layer in the SOI wafer bonding manufacturing method. SOITEC and SEH are examples of companies using this Smart cut/UNIBOND SOI bonded wafer manufacturing method (3).

In bulk Cz and epi wafer CMOS technology high energy ion implantation in the 2 to 3 MeV range is used to from deep triple wells for vertical well isolation, usually isolating the top p-well from the p-substrate inside a deep n-well (4). This triple well structure is typically used for DRAM, Flash and SRAM memory as well as embedded memory/logic circuits. Shallow trench isolation (STI) is the industry standard lateral isolation structure and improved isolation characteristics can be achieved through optimized deep retrograde well implantations as shown in figure 1 (5). Although high energy buried layer implant structures have been shown to improve latch-up they can degrade other device parameters (n-well to substrate leakage and breakdown voltage) and must be carefully integrated especially in order to achieve epi-replacement. To further increase device packing density, minimize lateral isolation spacing and improve (make more uniform) across wafer device electrical characteristics, non-shadowing implantation is needed (6). Shadowing can be completely eliminated through zero degree tilt implantation, however, a critical parameter for these implants is beam parallelism across the wafer to ensure uniform channeled dopant profile across the wafer. Figure 2 shows Rs non-uniformity across a 200mm wafer comparing batch implanter to single wafer implanter for zero degree tilt implantation. Due to the batch cone angle effect causing both wafer tilt and twist variation the batch implanter performance at zero tilt was 6% to 8% Rs variation while on the single wafer system it remained <0.5%. Dopant depth porfiles across wafers from a batch implanter showed both peak height and junction depth variations while the profiles from the single wafer implanter showed uniform channeling across the wafer with no peak nor junction depth variation (7). The batch non-uniform channeling can result in a large variation in device electrical performance across the wafer as reported by Kapila in reference 6.

HIGHER-k GATE OXIDE MATERIAL MODIFICATION

Embedded SOC devices require multiple (two or three) gate oxide thicknesses and one method reported to achieve this is through implanting various spieces (N, O, F and Ar) to enhance or retard silicon oxidation rate. Goto et al reported on using F implantation to enhance silicon oxidation rate by as much as 2x as shown in figure 3 while Togo et al reported up to a 5x reduction in silicon oxidation rate with N implantation and up to a 1.8x enhancement with Ar shown in figure 4 (8,9). An example of a system on a chip (SOC) where you have high speed CMOS (1.9nm oxide), low power CMOS (2.5nm oxide) and SRAM memory (5.0nm oxide) all on the same chip is shown in figure 5 from Goto. As thin gate oxides scale to below 2nm, gate leakage becomes an issue so higher-k gate materials are needed. Figure 6 shows gate leakage equivalent oxide thickness for silicon dioxide and oxynitride materials (10). Today the most advanced devices use oxynitride films, however, higher-k dielectrics will be needed at 70-100nm technology node. Due to problems with thermal and CVD higher-k material processing including oxynitrides and metal oxides a better manufacturing alternative is needed. These high-k amorphous deposited material re-crystallize at temperatures above 800C and they are also extremely sensitive to the silicon surface pre-clean treatment and surface residue (10). Therefore, a promising alternative method is gate material modification through implanting controlled amounts of selected impurities. Puchner et al reported on ultra low energy ion implantation of nitrogen into thin SiO2 between 10eV and 200eV to form oxynitride films and a plot of N implant energy versus depth into SiO2 is shown in figure 7 (11). Krug et al also reported nitrogen implantation between 3eV and 30eV into 1.0 nm oxides and Essaian et al reported implanting F into oxides to form low-k intermetal dielectric films with dielectric constants as low as 2.9 (12,13). This method also provides solution to integration issues such as low temperature processing and silicon surface pre-cleaning sensitivity since you start with a standard thermal SiO2 film.

CHANNEL & SOURCE/DRAIN ENGINEERING

Retrograde channels for improved SCE is now standard practice using In for Vt implantation or if the implant is done after gate stack formation using boron through gate implant (TGI) as reported by Ponomarev et al and shown in figure 8 (14). HALO implants also modify the device channel and SDE (source/drain extension) profiles to improve SCE and reduce Vt roll-off (15,16). Figure 9 shows the effects of high tilt HALO up to 60 degrees on SCE and Vt roll-off as reported by Miyashita et al (17).

The ITRS roadmap reports the need for ultra-shallow junction (USJ) for SDE with lower sheet resistance (Rs) as devices continue to scale. There has been some discussion and disagreement to the ITRS requirements for USJ at recent technical meetings including the April MRS-2000, Sept. SSDM-2000 and Sept. IIT-2000 meetings. Grossmann et al has shown in figure 10 that high Rs are acceptable to maintain the required device drive current (18). Similarly, Kim et al reported that the key contributor will be S/D contact resistance as you continue to scale and not SDE resistance as shown in figure 11 (19). However, if you still need to form USJ with low resistance for SDE, there are two basic techniques: 1) ultra low energy (sub-keV) implantation by beam-line or plasma implantation followed by high temperature short time annealing (RTA/spike or laser annealing) or 2) low energy (keV) implantation followed by low temperature SPE anneal. RTA/spike annealing will be used for 130nm technology and may be extended down to 100nm technology (20). Laser annealing on the other-hand has major process integration issues which may prevent its use ever. They include dopant solid solubility deactivation issues, control of localized wafer surface melting especially on patterned device wafers with multiple material and layered structures such as STI and gate poly material issues (21,22). Therefore, low temperature SPE looks to be the best long term solution for both ultra-shallow junction formation and high-k gate material process integration. Also, there has been several reports on solving the leakage issues with low temperature processing (23, 24). To date the state of the art Rs-vs-Xj results using low temperature SPE at <600^{o}C is shown in figure 12 (25, 26, 27). Note the limit from RTA anneals as first reported by Shichiuchi (26). To maximize implanter productivity these implants are done at zero degree tilt resulting in channeling. As described earlier in the isolation section of this paper, beam parallelism for uniform channeled dopant profile is critical and a 1 degree variation has been reported to cause as much as a 5% Vt shift. An example of 1% energy contamination is shown in figure 13 as reported by Murooka et al for a 500eV implant in drift versus decel mode (28). This 1 % energy contamination results in an 20% junction depth change. Lenoble et al showed channeling-vs- non-channeling profiles from implants into crystalline or PAI (pre-amorphous implant) wafers in figure 14 (29). Channeling was 36% deeper in the crystalline sample for the 1keV boron implants. Figure 15 shows channeling versus non-channeling profiles for a 2kV PLAD implant after 550^{o}C SPE. Using the 100nm ITRS node as a reference point, Osburn simulated the effects of implant dose, energy and angle variation and showed that tilt angle had the most significant impact for Vt shift at Lgate=65nm as shown in figure 16 (30). Al-Bayati showed that a 1% energy contamination results in 1% Vt shift (5mV), 2% Leff change (20.0nm) and 3% Idsat change (31).

PROCESS SIMPLIFCATION & MASK COUNT REDUCTION

The need of retrograde channels was described above however a new trend is to do this pre-gate Vt implant post-gate for process simplification and mask reduction was reported in reference 14 and it has been implemented into manufacturing by several companies around the world for 0.18um & 0.22um CMOS technology for logic and memory devices (32). When combined with high tilt SDE implantation, this PoGI (post-gate implant) process simplification can reduce up to 4 masking levels in twin well CMOS front end processing as shown in figure 17 (33). Two key factors in the PoGI process is high tilt high current SDE implant through the side-wall spacer and the Vt implant through the gate stack structure. The are numerous process simplification reports using high tilt implantation for SDE/LDD formation including Wang et al, Sultan et al, Takeuchi et al and Juang et al (34,35,36,37). Through gate implantation with disposable spacer processing for mask count reduction has also been reported by Horiuchi and Grossman et al (38,39). The high tilt SDE implant allows for precise positioning of the SDE structure for gate overlap control especially when using a notch poly gate (40,41,42).

NEW IMPLANT DESIGN EVOLUTION

For the last decade high current and high energy implanters were designed with a large disk capable of handling up to 18 200mm wafers per batch/load. Only medium current implanters were single wafer. This decade will see the transition to 300mm wafers and the concern with batch processing so single wafer high current and high energy implanters are now available commercially (high energy single wafer: VIISta-810 & 3000 and SWIFT; high current single wafer: VIISta-80 and VIISta-10 P^{2}LAD). A new implantation method called plasma implantation is also now available for very low energy implantation down to 20eV of various species for ultra-shallow junction dopant profiles and the new higher-k gate material modification application. This single wafer chamber design could lead to clustering implantation to other processing steps and this could dramatically change implanter designs in the future as shown in figure 18 (25).

SUMMARY

This paper discussed how the use of advanced ion implantation techniques is solving equivalent scaling issues in the areas of: 1) wafer and isolation engineering for improved device vertical and lateral isolation, 2) higher-k gate material modification to lower gate leakage, 3) channel and S/D engineering for shallow junction formation and gate overlap control, 4) PoGI process simplification and lithography mask count reduction and 5) new advanced ion implanter designs driven by 300mm wafers and new cluster tool possibilities.

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FIGURES

Figure 1: STI n+ trigger current latch-up results for various high energy retrograde well structures (5).

Figure 2: Batch versus single wafer implant Rs uniformity for various tilt angles (7).

Figure 3: Enhanced silicon oxidation rate with F implantation (8).

Figure 4: N and Ar implantation for silicon oxidation rate control (9).

Figure 5: Multiple (triple) gate oxide thicknesses for SOC (8).

Figure 6: Thin gate oxide leakage effects (10).

Figure 7: N implant into SiO2, energy versus depth (11).

Figure 8: Post-gate (TGI) Vt implant (14).

Figure 9: High tilt HALO implantation (17).

Figure 10: Optimized Rs-vs-Xj for drive current (18).

Figure 11: Scaling contact resistance (19).

Figure 12: SPE Rs-vs-Xj results (25, 26, 27).

Figure 13: 1% energy contamination profile (drift versus decel mode) (28).

Figure 14: Channeling profile (crystalline versus amorphous) (29).

Figure 15: PLAD channeling profile.

Figure 16: Vt shift sensitivity on dose, energy and angle variation (30).

Figure 17: PoGI process flow (33).

Figure 18: VIISta-10 P^2LAD (25).

KEY WORDS:

Channeling

Device Scaling

Gate Material

Ion Implantation

Plasma Doping

Post-Gate Implant

Process Simplification

Shallow Junction

Solid Phase Epitaxial Growth