Borland's Overview of the Latest in Intrinsic Gettering: Part II

In Part I, we reviewed the theory behind intrinsic gettering. Now we show you how to put it to work.

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When integrating intrinsic gettering (IG) into your CMOS device process flow, don't neglect how the IG is to be activated. It's critical in order to optimize and maintain IG effectiveness and durability through the numerous high temperature thermal anneals.[1,2]

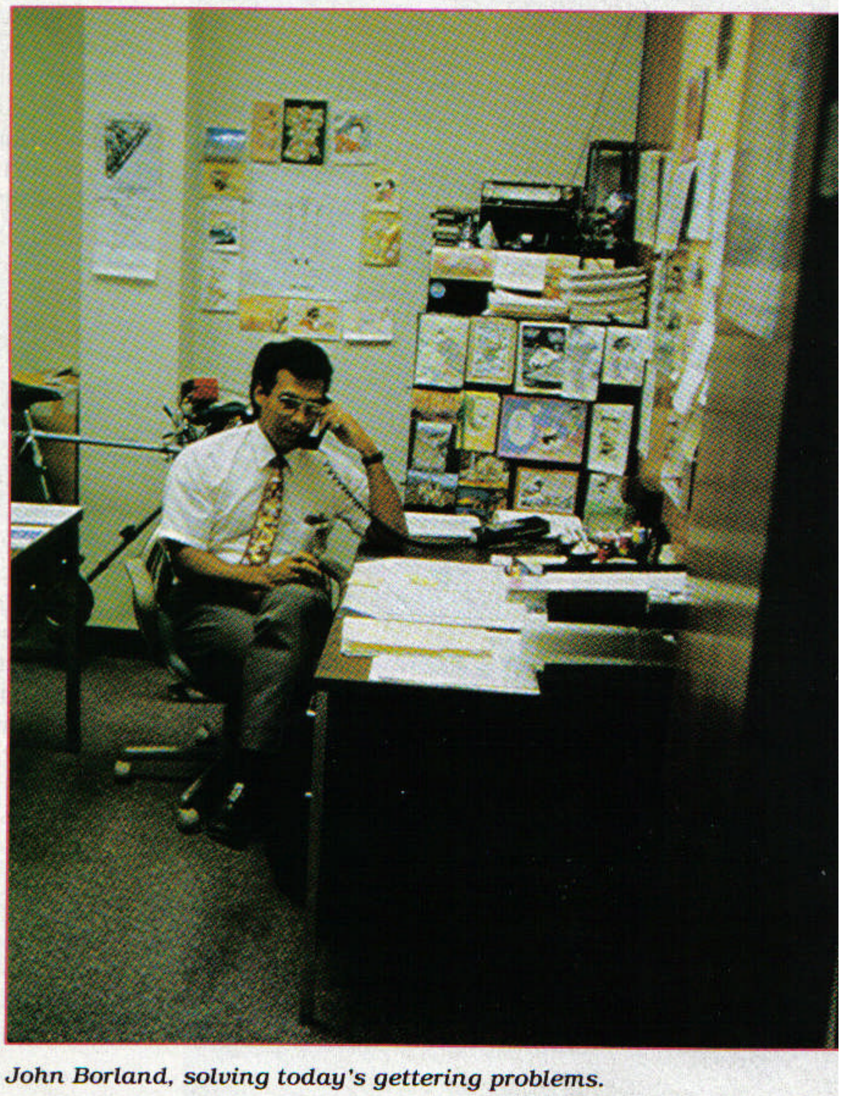
There are three techniques you can use to activate IG in a CMOS process:

- process induced,
- enhanced process induced, or
- pre-process induced.

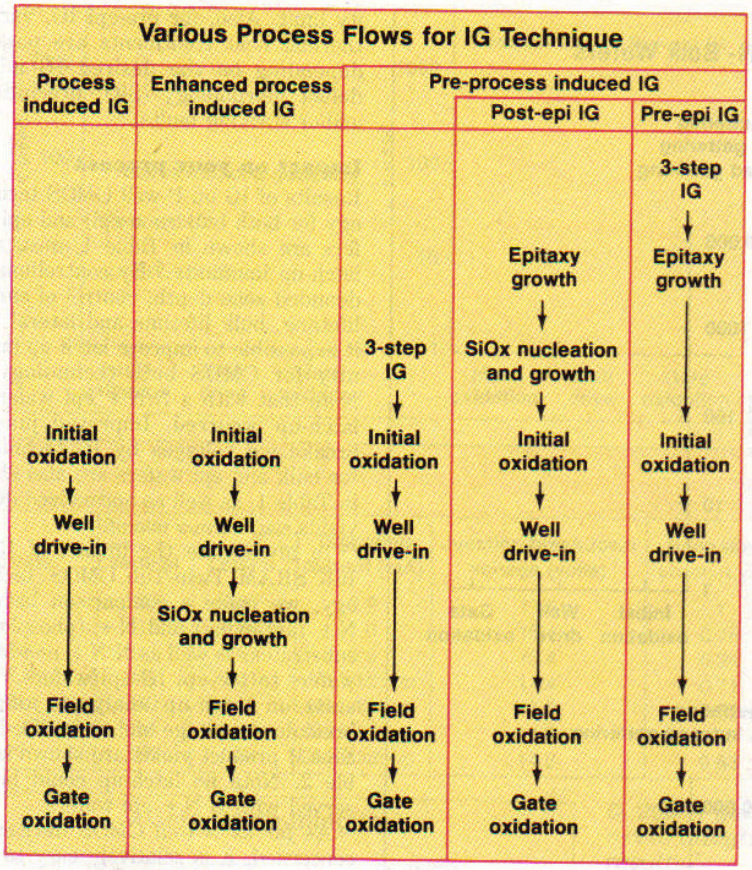
When using an epi wafer, two variations of pre-process induced IG are possible — either pre-epi or post-epi (Fig. 1).

In most CMOS device processing lines, process induced IG occurs naturally in the wafer because the processing thermal sequence is similar to the ideal 3-step thermal IG cycle (reviewed in Part 1, *SI* April, 1988). The high temperature (>1150°C) N-well/P-well drive-in process also acts as an effective denudation step, causing oxygen outdiffusion. Following the well drive-in process is usually the field oxide isolation process at intermediate temperatures between 900°C and 1000°C. This will also induce oxygen precipitation and growth in the bulk of the wafer, thereby activating the IG mechanism. You can clearly see this in Fig. 2 for a P/P+ epi wafer where process induced IG created a denuded zone with bulk micro-defects.

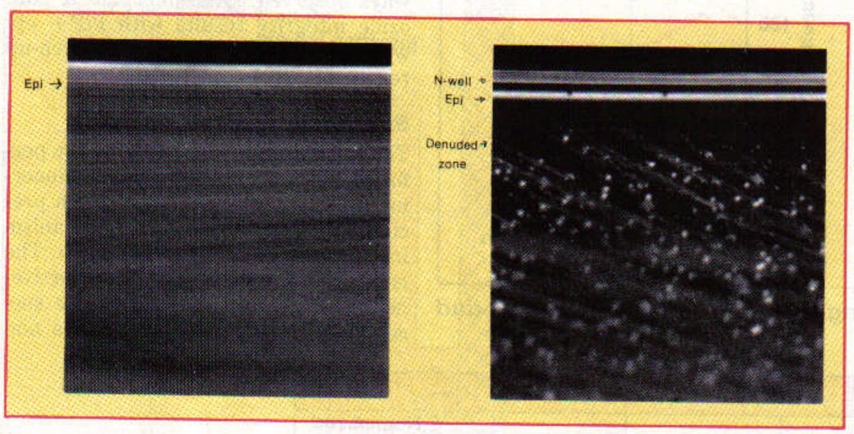
For some other CMOS device processing lines, process induced IG may not be sufficient, so enhanced process induced IG is required. You can easily achieve this by adding a 700°C SiO_x nucleation anneal step after the well drive-in step, prior to the field oxide isolation



John Borland, solving today's gettering problems.



1. Various techniques you can use to integrate IG into the CMOS process flow.



*2. P/P+ epi wafer showing process induced IG (**a**) after initial oxidation and (**b**) after gate oxidation.[17]*

step. This results in an increase in precipitate density and precipitation rate during the field oxide isolation anneal. In this way, the IG effectiveness is improved, especially for the critical gate oxidation step.

Pre-process induced IG

If neither process induced IG nor enhanced process induced IG is efficient enough, pre-process induced IG may be required. Subjecting the wafer to the 3-step IG cycle will achieve this — by inducing denudation, SiO_x nucleation and precipitate growth for IG activation — prior to introducing the wafer to CMOS device processing.

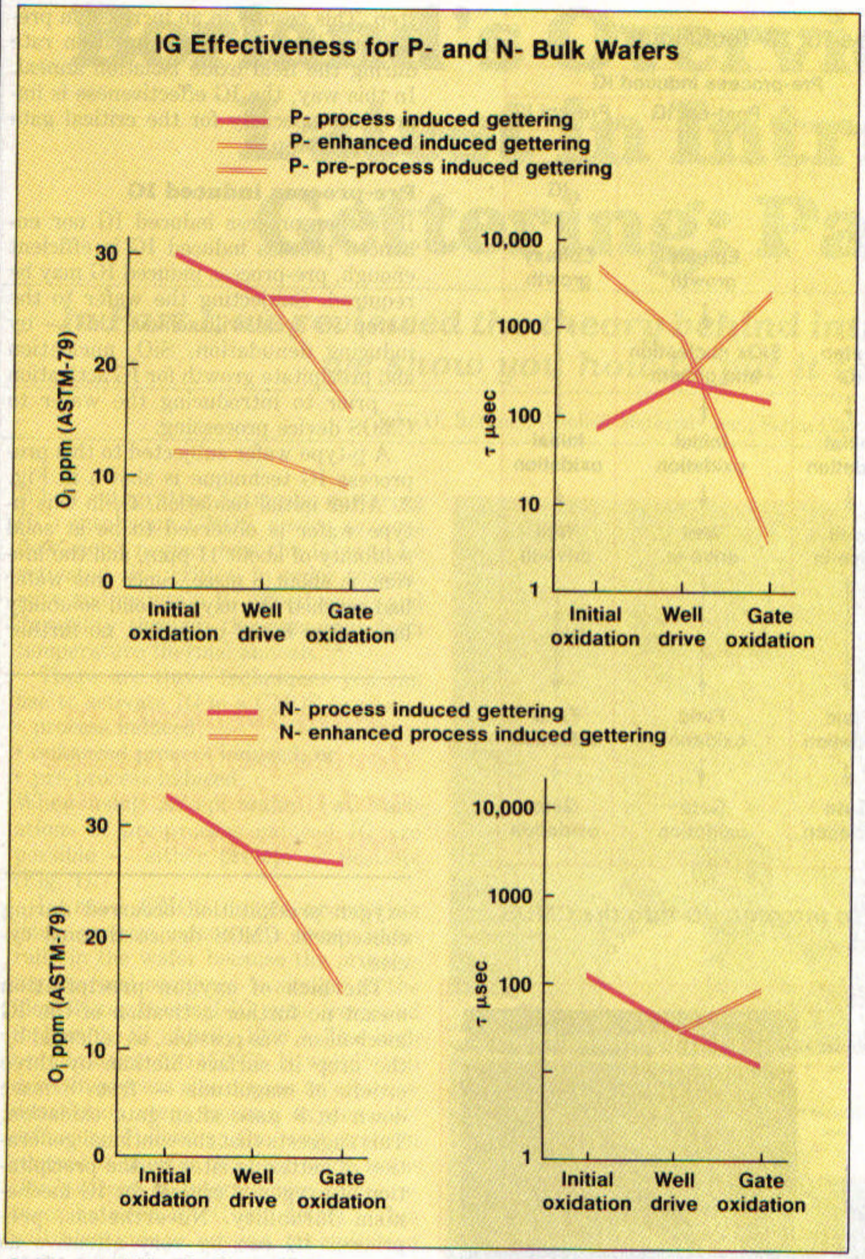
A p-type wafer subjected to this pre-process IG technique is shown in Fig. 3. After initial oxidation, O_i in this p-type wafer is observed to be at solid solubility of about 11 ppm, and the lifetime is about 8 msec. Since this wafer had reached the oxygen solid solubility limit after initial oxidation, no further

...improvements in device performance and yields were always observed.

oxygen precipitation occurred during subsequent CMOS device thermal cycles.

The lack of oxygen precipitation meant no further activation of the IG mechanism was possible, as reflected by the drop in surface lifetime by three orders of magnitude — from 8 msec down to 8 μsec after gate oxidation. This suggests that the continual generation of gettering sites by the precipitation of oxygen is critical for IG mechanism durability. Nevertheless, pre-process IG can be very effective as shown in Fig. 4 for P/P+ and N/N+ epi wafers which were subjected to both pre-epi IG and post-epi IG. For P/P+, the best results were with the pre-epi IG technique. For N/N+, the best results were with the post-epi IG technique.

The lifetime degradation trend in the post-epi IG P/P+ wafer is believed to be due to a lack of continual oxygen precipitation in the P+ substrate. This was observed in the P− wafer (Fig. 3), having reached the oxygen solid solubil-



3. P− and N− bulk wafers comparing O_i and τ for IG effectiveness and durability.[18]

ity limit. Also, for pre-epi IG, various thermal heat treatments are possible depending on the desired IG microdefect morphology (SiO_x precipitates and/or stacking faults).[1]

Impact on your process

Results of IG on P-well CMOS technology for both bulk (non-epi) and epi wafers are shown in Table 1, measuring latch-up immunity.[3] By controlling the denuded zone depth, control of surface lifetime, bulk lifetime and lateral beta it is possible to improve latch-up immunity for CMOS bulk technology.[3,4,5] Note that with a N/N+ epi wafer, no latch-up occurred. Improved junction breakdown voltages by IG techniques for bulk and epi wafers are also shown in Table 1, as well as normalized device yields.

To investigate the impact of IG on 16K SRAM Twin-Tub CMOS Technology, we made a comparison between N+ (antimony) and N+ (phosphorus) substrates, as well as N/N+ non-IG epi wafers to pre-epi IG epi wafers.[6,7] Results on latch-up analysis, junction breakdown voltage and normalized 16K SRAM product yields are shown in Table 2. Note no latch-up could be observed with N/N+ epi wafers.

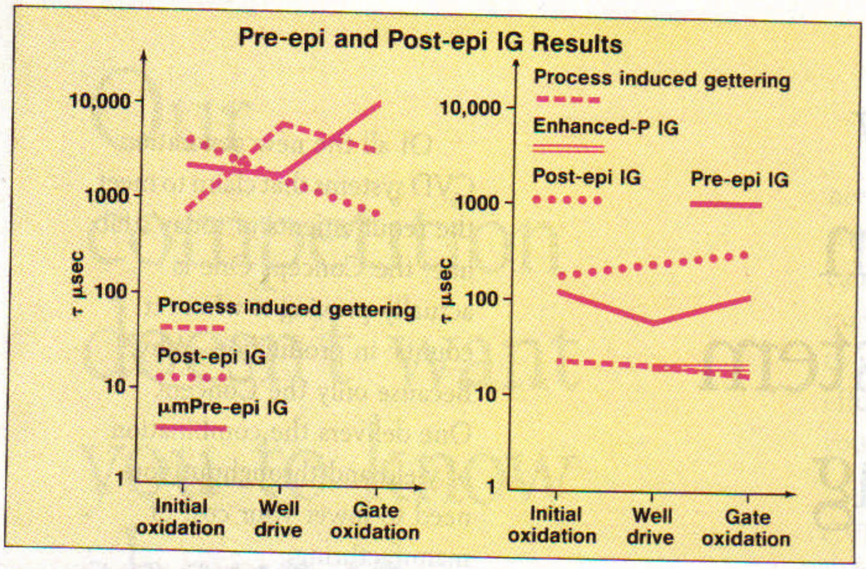
As far as N-well CMOS devices are concerned, it is relatively easy to activate the IG mechanism in P/P+ epi wafers. As a result, improvements in device performance and yields were always observed.[8] Excellent 200 Å gate oxide integrity results with P/P+ epi wafers are shown in Fig. 5 and latch-up results are shown in Table 3.[9,10]

Summary

The key to improving CMOS device performance and yield is proper engineering and integration of the oxygen precipitation intrinsic gettering mechanism into the CMOS device process line. The end result is improved getter effectiveness and durability. This can be successfully achieved in bulk wafers and

Table 1. Device Performance and Yield

	B_V	B_L	I_H (mA)	N+ to P-well	P+ to substrate	Normalized yield
N-bulk	60	0.18	20	15.5 = 3.5	45.4 = 10.4	1.0
N-bulk IG	52	0.22	40	16.6 = 2.9	41.8 = 10.0	1.75
Epi	48	0.21	No latch-up	12.7 = 3.9	41.9 = 13.6	0.0
Pre-epi IG	50	0.16	No latch-up	16.3 = 3.3	43.6 = 9.3	0.75
Post-epi IG	50	0.21	No latch-up	16.8 = 4.8	44.4 = 13.4	

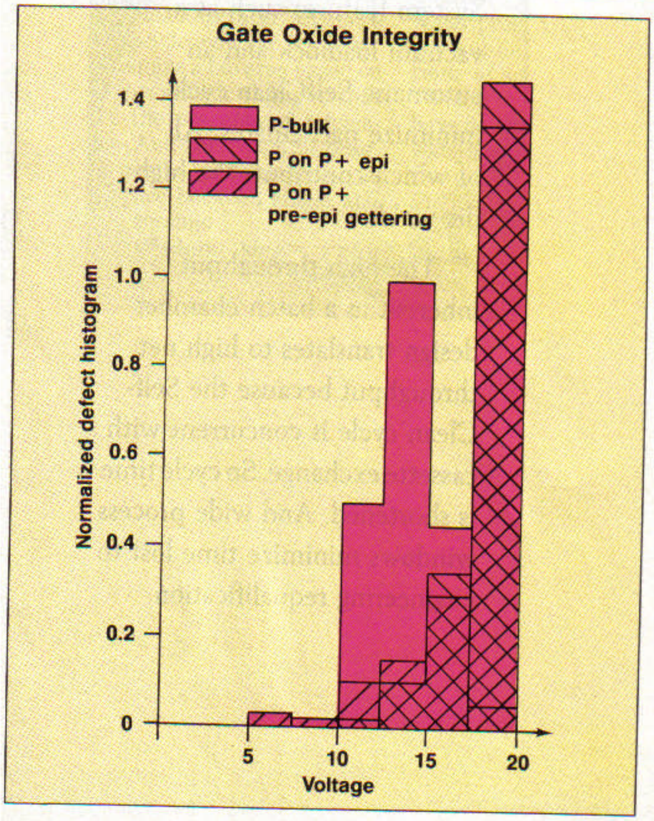


*4. Pre-epi and post-epi IG results for **(a)** P/P+ and **(b)** N/N+.*[18]

epi wafers by using process induced IG, enhanced process induced IG or pre-process induced IG techniques. □

Table 2. Summary of Parasitic Bipolar Current Gain and Triggering Current

Substrate	Bipolar current gain: Vertical	Bipolar current gain: Lateral	Triggering current (mA)	Junction breakdown voltage (volts)	Normalized product yield
N−	293	0.87	0.9	17.5	1
N/N−	313	0.80	1.0	16.1	0.76
IG N/N−	311	0.67	0.9	13.4	0.29
N/N+ (P)	349	1.41	No latch-up	14.4	0.71
IG N/N+ (P)	340	1.31	No latch-up	17.5	0.92
N/N+ (SB)	354	1.15	No latch-up	14.2	0.69
IG N/N+ (SB)	350	1.24	No latch-up	14.8	0.83



5. 200 Å gate oxide integrity results.[7]

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Table 3. N-well Latch-up (1.25 µm design rules)

	B_V	B_L	I_H (mA)
P-bulk	24.8	2.2	4.4
Epi	27.6	5.0	7.3
Pre-epi IG	25.4	5.2	12.4

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