Borland's Overview of the Latest in Intrinsic Gettering: Part I

In the first of a two part series, the maven of intrinsic gettering describes the fundamental mechanisms and how they are affected by key process variables.

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Process induced defects and contamination are almost unavoidable during CMOS device fabrication, due to the numerous thermal treatments wafers go through. This is equally true for wafers of "bulk" silicon and wafers with epitaxially grown silicon.

If these defects or impurities are located in the device active region, they can, of course, hinder device performance and lower device yield. By locating them in the inactive regions of the material, however, you can actually use them to *improve* device performance![1-3]

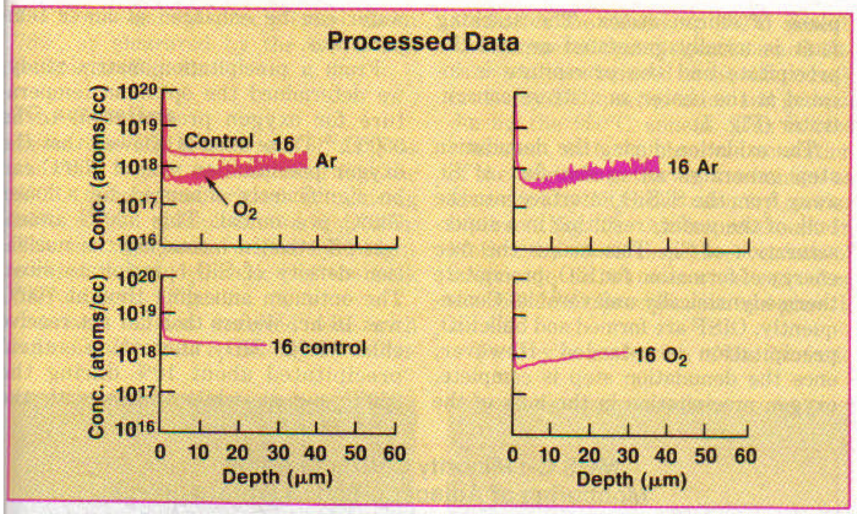
Specifically, with the intrinsic gettering (IG) technique, the intrinsic material properties of Czochralski (Cz) grown silicon wafers (e.g., interstitial oxygen, substitutional carbon, silicon-vacancies, silicon-interstitials, dopant point defects, as grown precipitates and stacking faults, etc.) are used to induce bulk oxygen precipitation by the formation of SiO_x complexes. These SiO_x precipitates generate silicon lattice disorders and dislocations that act as gettering sites (traps) for unwanted impurities. Also associated with the formation of SiO_x precipitates is the ejection of silicon interstitials (Si_I), which can enhance the migration/diffusion of the impurities to the gettering sites.

Several reports have examined how IG techniques can improve both device performance and yield in CMOS bulk and epi wafers.[4-9] However, the IG technique must be optimized to maintain gettering effectiveness and durability during processing. This month, I will describe the fundamentals of intrinsic gettering — how it works in both bulk and epi silicon, and its dependence on process variables such as pre-anneal temperature and doping. In Part 2, I will show you how to integrate the IG technique into your CMOS processes.

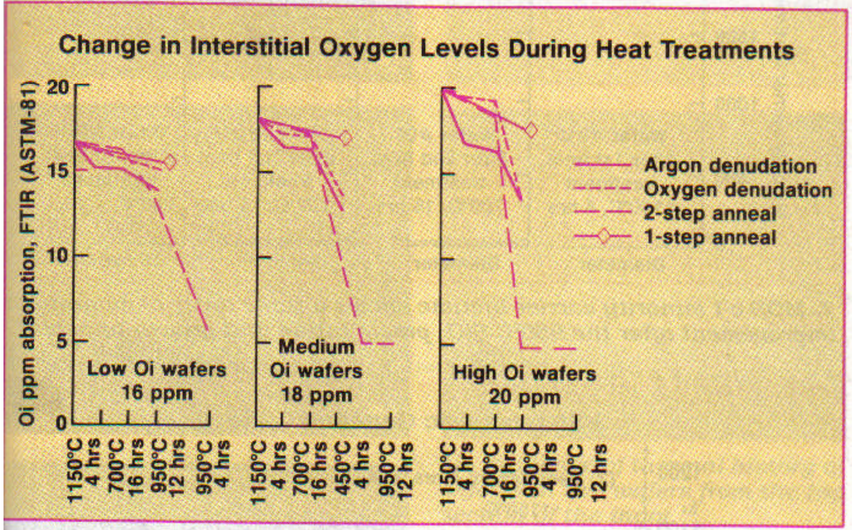
John Borland, sporting his favorite Chinese dragon tie.

Denuded zone formation

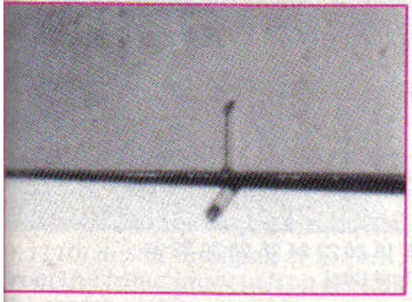
For effective IG, both a denuded zone (defect free area) in the device active region and gettering sites in the bulk of the wafer must be formed.[10-12] The denuded zone is created by a high temperature heat treatment that causes oxygen atoms — interstitial oxygen (O_I) — to out-diffuse from the wafer surface, resulting in a region near the surface that is depleted of oxygen. A few hours of heat treatments at temperatures above 1100°C, in inert or oxidizing ambients, is very effective for denuding. Examples of the oxygen out-diffusion profile for argon and oxygen ambient denudations are shown in Fig. 1, as



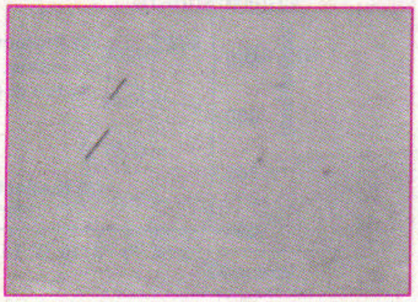
1. SIMS analysis shows oxygen depletion in the denuded zone. Note that the oxygen profile from the oxidizing ambient sample shows no evidence of O^{16} scatter, while the argon ambient sample shows significant amounts.[11]



2. Change in O_I during heat treatments, as measured by FTIR.[11]



3. OISF at surface in ~~(110)~~ (100) and (110) planes.[11]



4. Argon ambient denudation with bulk stacking faults.[11]

measured by secondary ion mass spectroscopy (SIMS).

A surface oxide cap is recommended to protect the surface from possible contamination and pitting. But a pure oxidizing ambient is *not* recommended because, during the high temperature oxidation, excess Si_I are ejected at the oxidizing front. This can lead to oxidation induced surface stacking faults (OISF).

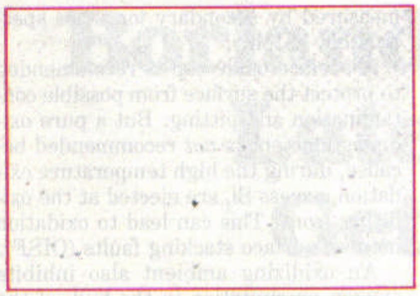
An oxidizing ambient also inhibits oxygen precipitation in the bulk of the wafer. This is shown by SIMS in Fig. 1, and further illustrated by FTIR measurements in Fig. 2. The FTIR measurements track O_I concentrations and changes in O_I (ΔO_I), for various denudation ambients.[13]

The SIMS oxygen (O^{16}) profile for the oxidizing ambient sample shows no evidence of O^{16} scatter. The argon ambient sample, however, shows significant O^{16} scattering in the bulk of the sample, signifying evidence of oxygen precipitation. The FTIR measurements also show evidence of oxygen precipitation in the bulk of the wafers. A ΔO_I of 3.5 ppm was observed in the argon ambient annealed wafer, while a ΔO_I of <1.0 ppm was observed in the oxidizing ambient annealed wafer.

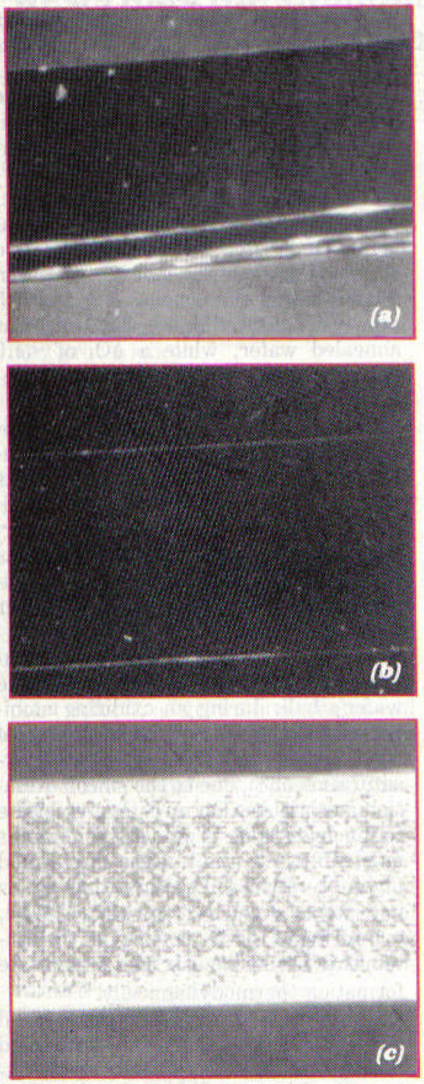
Cross-sectional cleaved (110) photomicrographs after Wright defect etching shows only surface stacking faults with no bulk micro-defects for the oxidizing ambient wafer (Fig. 3). No surface defects — only bulk micro-defects and bulk stacking faults — were observed for the argon ambient wafer (Fig. 4).

We can explain the retardation/inhibition of oxygen precipitation in the wafer's bulk during an oxidizing ambient denudation — and the formation of surface stacking faults — by the supersaturation of Si_I due to the silicon oxidation mechanism. For an SiO_x precipitate to nucleate and grow, oxygen atoms must diffuse to the nucleation site and favorably form Si-O alternating bonds in a partially coherent structure. Also, a lowering of the free energy of the system (ΔG) is required for SiO_x precipitate formation thermodynamically.[14]

As oxygen atoms are incorporated into the SiO_x matrix, Si_I are generated and ejected due to the volumetric expansion of the silicon lattice as the SiO_x complex forms. Ejected Si_I atoms migrating away from the precipitate can build up sufficient energy to form an extrinsic bulk stacking fault: an extra



5. *Stacking fault formed around an SiO_x precipitate.*[10]

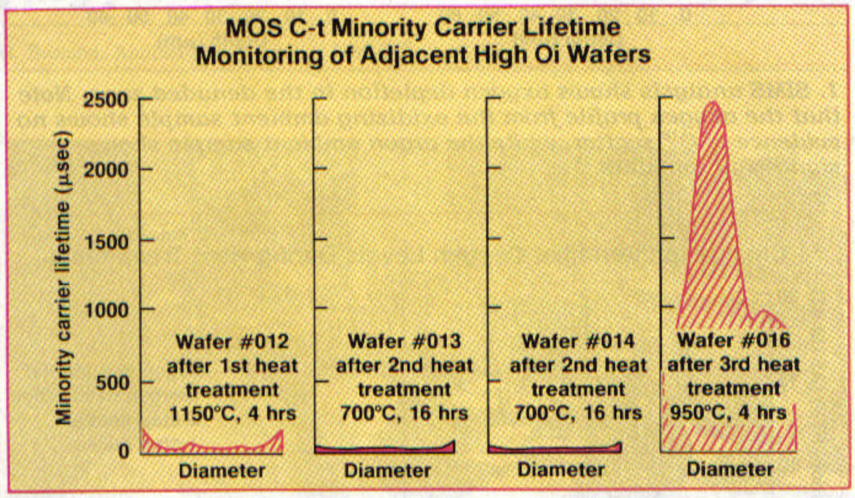


6. *(110) cross-sectional micrographs defect etched* ***(a)*** *after denudation step,* ***(b)*** *after SiO_x nucleation step, and* ***(c)*** *after precipitate growth step.*[10]

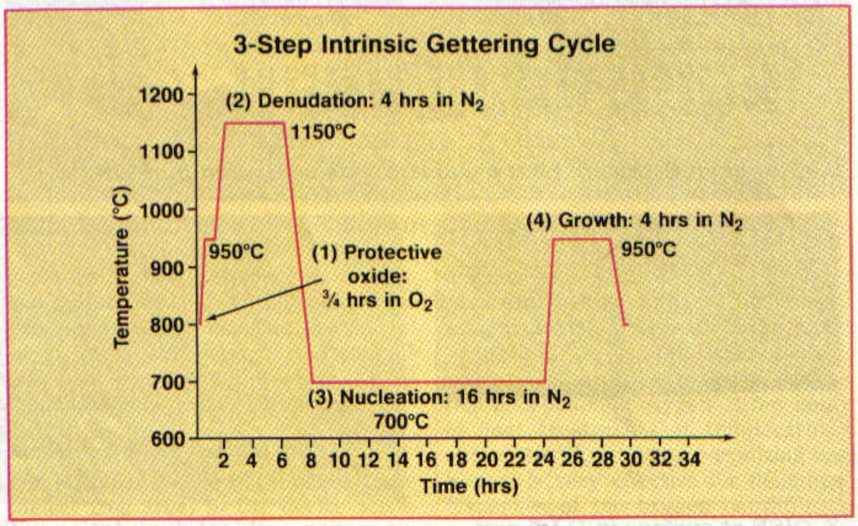
plane of silicon atoms. The stacking fault is usually generated around the precipitate and the precipitate is located at the center as a stress concentrator (Fig. 5).

The oxidation during the denudation step generates an excess flux of Si_I away from the Si/SiO_2 interface into the bulk of the wafer, resulting in a supersaturation of Si_I. This makes the free energy of formation for SiO_x precipitate thermodynamically unfavorable. Consequently, OISF are formed and bulk SiO_x precipitation is retarded. However, once the denudation step is complete, oxygen precipitation in the bulk of the wafer can be enhanced at lower temperatures.

From a precipitation matrix study, we determined the optimum temperature for oxygen precipitation to be 950°C.[15] These results showed that the oxygen precipitation rate at 950°C can be significantly enhanced by a lower 700°C pre-anneal. This 700°C anneal was effective in increasing the nucleation density of SiO_x precipitate sites. The optimum annealing time at 700°C was 16 hr. Wafers that did not receive this 700°C SiO_x nucleation anneal precipitated about 10% during the 950°C anneal, while wafers with the



7. *MOS c-t minority carrier lifetime shows a three order of magnitude improvement after the 950°C SiO_x precipitation and growth anneal.*[10]



8. *For effective IG, this 3-step IG thermal cycle is ideal.*[17]

700°C pre-anneal precipitated about 78%, as measured by the ΔO_I FTIR technique (Fig. 3).

IG activation

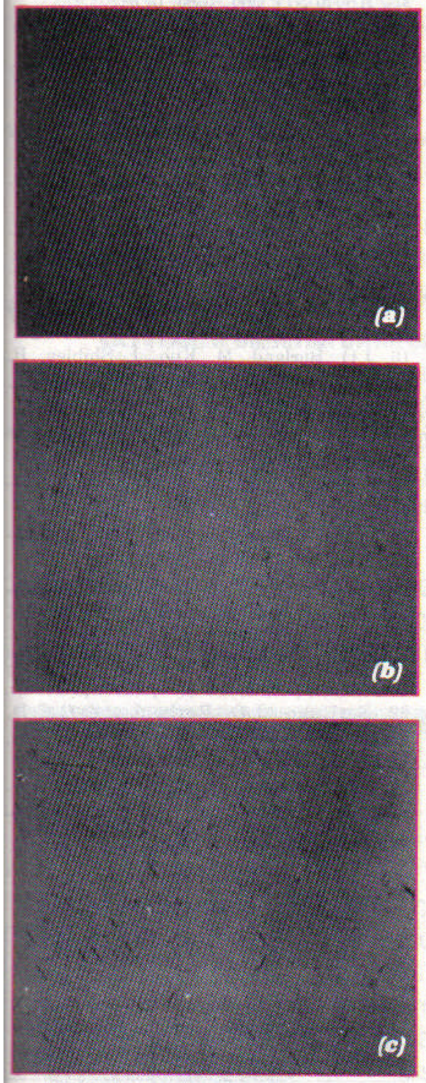
From the FTIR analysis of ΔO_I, as shown in Fig. 3, we concluded that the 950°C anneal was critical in inducing bulk oxygen precipitation and growth. This has also been verified by Wright etchant defect delineation of the bulk micro-defects (Fig. 6).

A well defined denuded zone with bulk micro-defects could only be delineated after the third step 950°C anneal. This suggests that dislocations and lattice strain are induced in the silicon bulk lattice by SiO_x precipitation and growth during the 950°C anneal. This is also consistent with the observed activation of the intrinsic gettering mechanism as measured by MOS C-t minority carrier lifetime (Fig. 7). An improvement in lifetime by more than three orders of magnitude ($>10^3$) was observed after the 950°C SiO_x precipitation and growth anneal.

The key to activation of the intrinsic gettering mechanism is SiO_x precipitation and growth. However, the presence of a denuded zone is also important. The ideal three-step thermal cycles required for effective IG are:

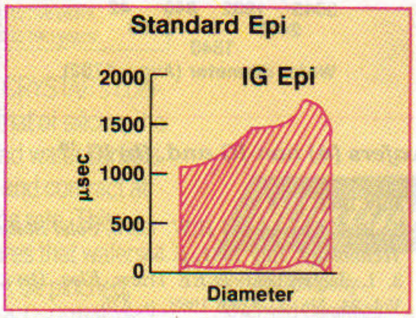
- denudation for oxygen out-diffusion,
- SiO_x nucleation, and
- SiO_x precipitation growth (Fig. 8).

It's also important to note that the silicon intrinsic material properties are controlled by Cz crystal growth conditions.[16-18] Wafers from different locations on the same crystal ingot will have different intrinsic material properties and precipitate differently (Fig. 9). Also, wafers from different vendors will precipitate differently, and differences in wafer thermal histories will alter the intrinsic material properties. The latter can result in different bulk micro-defect morphology (SiO_x precipitates and/or stacking faults) shown in Fig. 10.



*9. (110) defect analysis of wafers from the same ingot **(a)** top section **(b)** center section and, **(c)** bottom section.*[18]

10. Influence of thermal history of defects in two wafers from the top section of the ingot.[18]



11. MOS c-t lifetimes for P/P+ epi wafers non-IG.[16]

Epitaxial IG

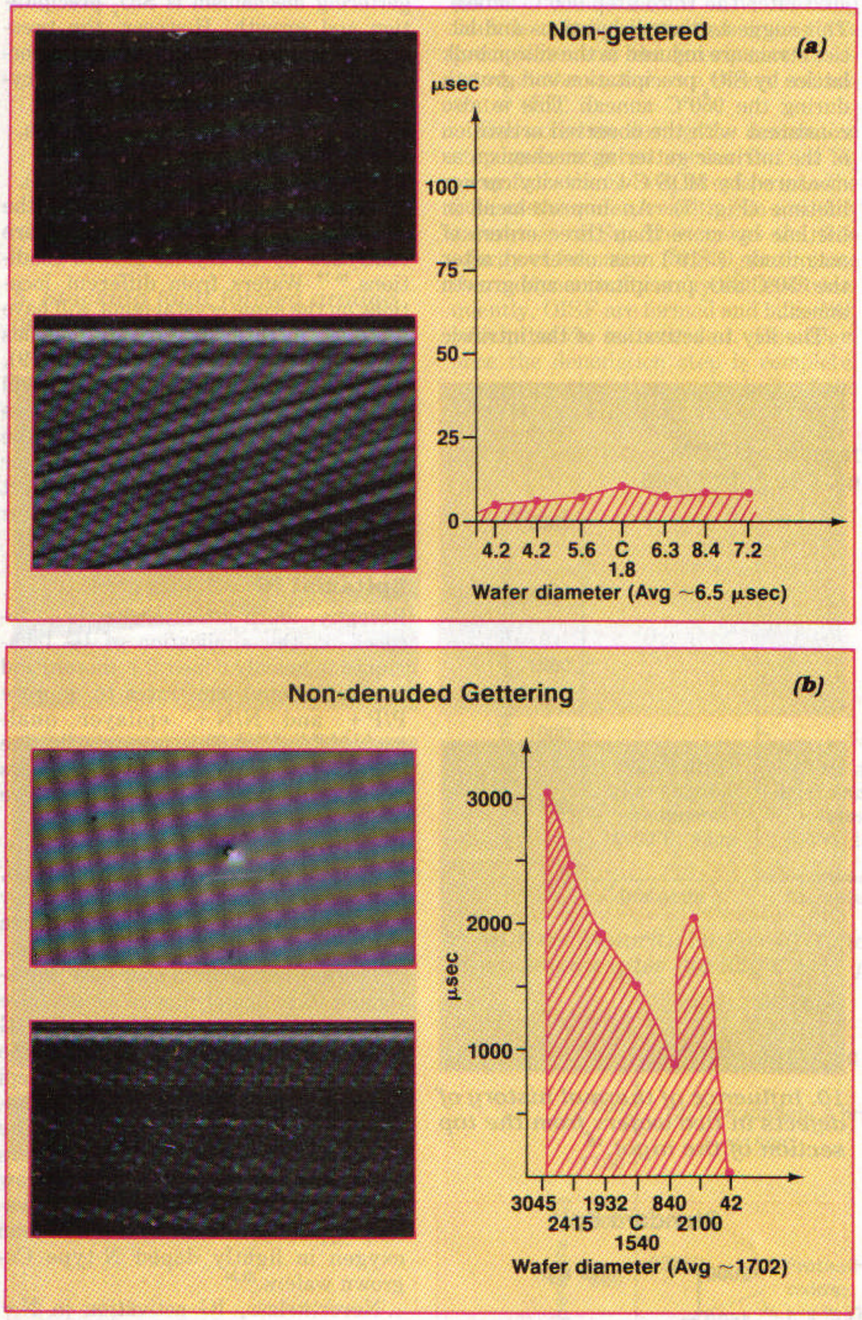
Recently, much attention has been focused on the application of IG techniques to heavily doped P+ (boron) and N+ (antimony) substrates to improve P/P+ and N/N+ epilayer quality.[5,7,8,9,16,17,18,20,21] This is primarily due to the increased popularity in epi wafers for CMOS device technology where latch-up prevention is important.

Although the use of P/P+ and N/N+ epi wafers will prevent CMOS latch-up, the quality of the epilayer will directly affect other device parameters that can degrade device performance and yield.

The few researchers that have investigated IG in heavily doped wafers have described the ease of activating the IG mechanism in P/P+ epi wafers, and the difficulty of IG activation in N/N+ epi wafers whether the N+ doping was antimony, phosphorus or arsenic.[19,22] The inhibition of IG activation in N+ wafers has been reported to be due to the low oxygen content in Cz-grown N+ wafers: typically 20% to 60% lower than oxygen in lightly doped N-type Cz-grown wafers.[23,24]

Nevertheless, IG activation in N+ wafers have been successfully achieved either prior to, or after, epitaxial growth by applying pre-epi IG or post-epi IG techniques. A comparison between non-IG and IG epi wafers is shown in Fig. 11 for P/P+, and Fig. 12 for N/N+ epi wafers. Note the improvement in epilayer lifetime by 10^3 times.

The advantages of using intrinsic get-



*12. MOS c-t lifetimes for N/N+ epi wafers (**a**) non-IG and, (**b**) IG.*[16]

tering techniques for CMOS bulk and epi technologies should now be clear. In Part 2 of this series, you will learn how to integrate these techniques into your process line. □

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