NOVEL DEVICE STRUCTURES BY SELECTIVE EPITAXIAL GROWTH (SEG)
(INVITED PAPER)

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ABSTRACT

In the last few years, great interest has been generated in the selective growth of single crystal silicon in seed windows of an SiO_2 mask in order to fabricate novel device structures for VLSI/ULSI device technology. This increased interest in selective epitaxial growth (SEG) and its derivitives, simultaneous single/poly deposition (SSPD) and epitaxial lateral overgrowth (ELO) have led to several key processing breakthroughs that are currently changing the future direction and usage of silicon epitaxy. This paper will describe: 1) the key SEG processing breakthroughs that have occurred over the last 25 years, 2) some of the current limitations still observed with SEG processing and, 3) some of the novel device structures that are possible through the use of SEG techniques.

INTRODUCTION

SEG was first reported in 1962, by Joyce and Baldrey using $SiCl_4$ at 1200°C, atmospheric pressure (1). However, significant processing breakthroughs did not occur until the use of reduced pressure epitaxial growth (<80 torr) at low temperatures (<1000°C) in the SiH_2Cl_2 + H_2 + HCl system as first reported by Tanno et al in 1982 (2). Use of low temperature/low pressure (LT/LP) SEG processing conditions have resulted in: 1) improved epi surface morphology and planarity (3, 4, 5), 2) improved selectivity (6, 7), 3) reduction in Si/SiO_2 sidewall interface defects (7, 8, 9), 4) reduction in the in situ pre-clean temperature thus eliminating oxide lifting and undercutting (6) and, 5) improved epi thickness uniformity for different Si/SiO_2 ratios and window sizes (5, 10). Additional advancements are the use of a sacrificial oxide to improve SEG material quality (6, 11) and the use of <100> sidewall oxide orientation to eliminate sidewall defects and faceting (4, 6). Further improvements to the Si/SiO_2 sidewall interface has been observed through post-SEG oxidation to seal and enhance the Si/SiO_2 bonding (4).

CURRENT LIMITATIONS AND SOLUTIONS

Although there have been significant breakthroughs in SEG process development over the last 5 years, there are still some observed issues associated with SEG processing that must be resolved before it is widely accepted in production. These deal with the Si/SiO_2 sidewall interface and relate to enhanced sidewall junction leakage, as shown in Fig. 1 (7, 8, 12, 13) and sidewall inversion causing a "kink" effect in the n-channel device subthreshold characteristics, as shown in Fig. 2 (4, 8, 12, 13, 14, 15). An improvement in sidewall leakage has been observed by Stivers et al by going to lower SEG deposition temperatures (875°C, at 25 torr pressure) (12). This has also been reported by Matsumoto, and he correlated this effect to a significant reduction in the Si/SiO_2 sidewall interface defect by lowering the SEG deposition temperature from 1000°C down to 875°C (7). Elimination of the Si/SiO_2 sidewall inversion and n-channel device "kink" effect is possible through proper SEG sidewall doping control as shown by Manoliu and Borland (13).

Another concern associated with SEG is the corner faceting along the <100> direction. This faceting effect can be minimized and eliminated by optimizing the SEG growth conditions and device layout design. These have been shown by Ting et al (4), Borland et al (14), Stivers et al (12), Manoliu and Borland (13), and Matsumoto and Borland (16).

APPLICATIONS FOR NOVEL (ADVANCED) DEVICE STRUCTURES

In spite of these limitations, novel MOS, bipolar and BiCMOS device structures

have been achieved through the use of SEG processing.

Lateral Isolation

One attractive area for SEG application is lateral device isolation for CMOS, bipolar and BiCMOS technology. An important benefit of SEG isolation is its scalability which is well below the line width resolution of current production lithographic equipment. Kasai et al showed a CMOS structure where the n-channel and p-channel devices are isolated by an SEG structure 0.25 micron wide, 4.0 microns deep as shown in Fig. 3 (17). SEG is also being used to refill deep trench isolation structures for high speed bipolar and BiCMOS devices see Fig. 4 (18, 19). This SEG refilling technique is very attractive because it is insensitive to the trench profile resulting in planar refill. Also, it is free of void formation and can refill varying trench widths simultaneously.

Selective Doping

Another attractive application of SEG is in the formation of selectively doped n-type and p-type silicon/epi structures or silicon/epi structures of different doping concentrations. Independent N-well and P-well CMOS structures with retrograde wells can be formed as shown in Fig. 5 without the use of ion implantation and high temperature thermal heat treatments through graded epi techniques or buried layer epi techniques (6, 20). Also, independent bipolar npn and pnp transistors can be formed by SEG as described by Matsumoto (7), and for BiCMOS applications, independent bipolar and CMOS device doping levels are possible as described by Favreau (21) and Oh et al (22). SEG has also been used to form thin bipolar base structures and sidewall base contact bipolar transistors (Fig. 6) (23, 24). Another unique structure is shown in Fig. 7 where SEG was used to heavily dope the sidewall of a 4 Mega Bit DRAM trench capacitor cell structure (25).

Selective doping is also very attractive for SEG usage in back-end device processing for shallow junction formation (CMOS source/drain and bipolar emitter) and self-aligned contact refill and planarization for interconnect. Fig. 8 shows a selective heavily phosphorus-doped SEG structure for self-aligned source/drain contact refill and planarization for a 1 Mega Bit SRAM device (26, 27). This approach gives excellent contact yields and is not troubled by problems seen with selective tungsten such as contact/substrate interface properties (native oxide removal), shorts due to worm tunneling defects and metal surface morphology. PMOS source/drain contact refill can be accomplished by using the independent selective (n-type/p-type) doping described in Fig. 5. Bipolar shallow emitter formation and contact refill are also possible.

Silicon On Insulator

The third area for application of SEG and its derivitives are in the formation of 3-D silicon on insulator (SOI) structures. Two proposed 3-D SOI DRAM cell designs using SEG techniques are shown in Fig. 9 (28, 29). The SEG structure shown in Fig. 9A is used as a plug refill and the seed for the lateral recrystallization of the polysilicon material while in Fig. 9B, the SEG structure is used to form the vertical transistor. Also, elevated source/drain SOI structures are possible by simultaneous single/poly deposition (SSPD) as shown in Fig. 10 where polysilicon is selectively deposited over an oxide and single crystal silicon is selectively deposited over the exposed silicon regions (14, 30). A totally isolated SOI structure is shown in Fig. 11 using Epitaxial Lateral Overgrowth (ELO) (14).

SUMMARY

In summary, significant breakthroughs have occurred in SEG processing using low temperature/low pressure (LT/LP) epitaxial growth techniques. This has resulted in the successful application of SEG for many new advanced device structures. Despite some observed problems which still must be overcome, SEG holds great promise for next generation devices where device scaling and minimization of total processing steps are major challenges.

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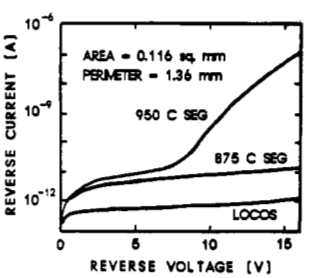

Fig. 1

Reverse characteristics of square N+/P junction diodes (12).

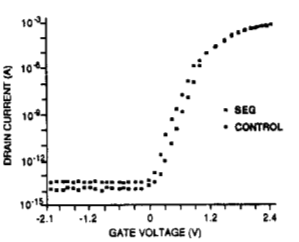

Fig. 2

Subthreshold characteristics of 50/3 n-channel transistors (12).

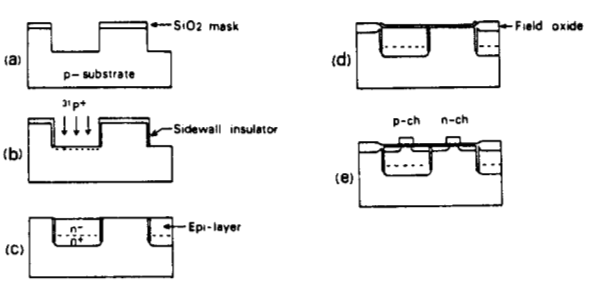

Fig. 3 SEG isolation structure 0.25μm wide, 4μm deep (17).

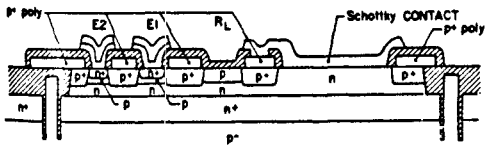

Fig. 4 High speed bipolar SEG refill trench isolation structure (19).

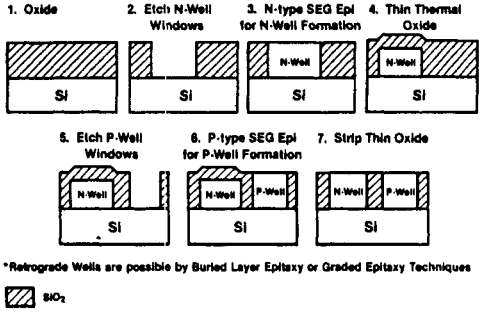

Fig. 5 Independent N-well, P-well formation by SEG (6).

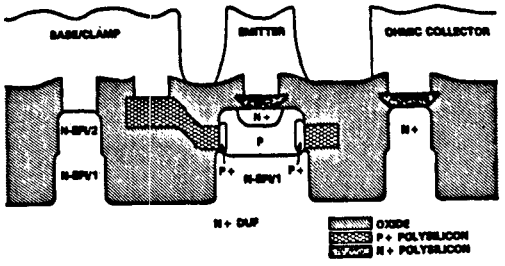

Fig. 6 Sidewall base contact bipolar transistor by SEG (24).

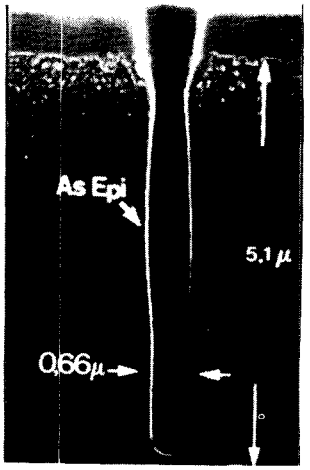

Fig. 7 4 Mega Bit DRAM trench capacitor sidewall doping by SEG (25).

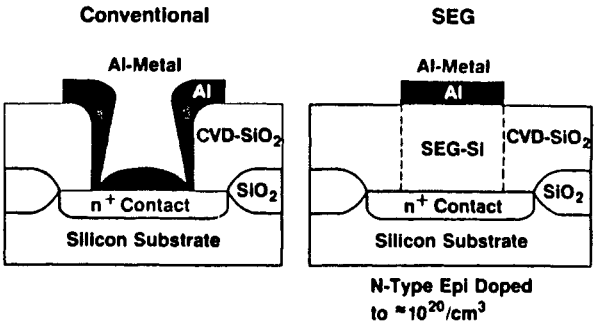

Fig. 8 1 Mega Bit SRAM self-aligned contact refill and planarization by SEG (26).

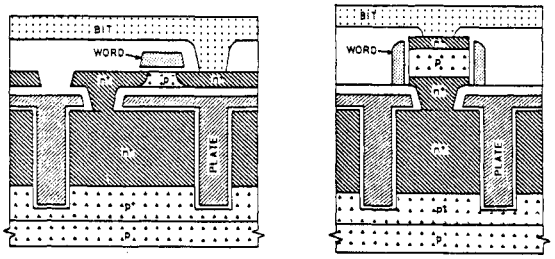

Fig. 9 3-D SOI DRAM cell by SEG (28).

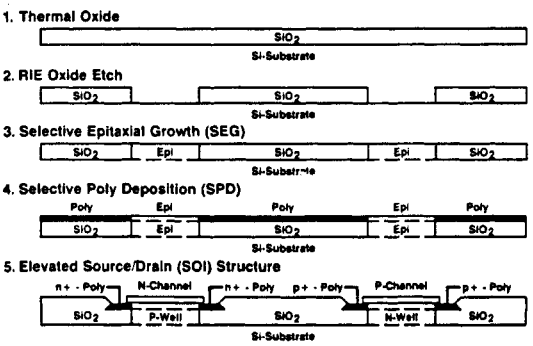

Fig. 10 Elevated source/drain SOI structure by SSPD (14).

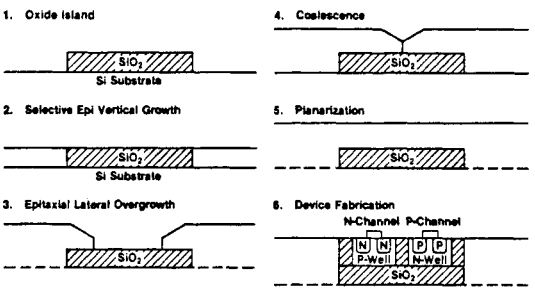

Fig. 11 CMOS SOI structure by ELO (14).