A SUBMICRON DUAL BURIED LAYER TWIN WELL CMOS SEG PROCESS

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ABSTRACT

This paper describes an advanced submicron CMOS process which uses selective epitaxy to successfully build high quality and high density CMOS transistors. The need for LOCOS is eliminated and devices are isolated by thick thermal oxide without the use of trenches. By properly combining processing parameters during epitaxial growth, optimum selectivity, faceting, and device characteristics are obtained. The device quality of the selectively grown epitaxial film is evidenced by high yielding ring oscillator circuits.

INTRODUCTION

An improved CMOS process which uses selective epitaxy to fabricate submicron CMOS transistors has been developed. Selective epitaxy has been proposed (1) to improve the isolation and density of CMOS circuits. Previously reported work showed non-optimal epitaxial film topography manifested in steep corner faceting. Device characteristics obtained were not adequate for ULSI type applications. This paper describes a dual buried layer SEG CMOS process which overcomes the drawbacks of other similar efforts.

PROCESS DESCRIPTION

The schematic cross-section and an SEM cross-section of a finished single layer metal CMOS device are shown in *Figure 1.* The process is built on 100 mm diameter p(100) silicon with oxide-silicon edges oriented in the <100> directions. A thick thermal oxide of 1.1 μm is grown and active p- and n- channel transistor areas are defined. Two independent heavily-doped boron and arsenic buried layers are then defined and implanted for the n- and p- channel transistors respectively. The selective epitaxial film was grown in an AMC-7810 radiantly-heated, low-pressure epitaxial reactor. A five-minute in-situ H_2 bake at 1000°C, and 25 Torr was used to remove the native oxide prior to deposition. The selective epitaxial growth (SEG) was done at 950°C, 25 Torr, in an H_2 + SiH_2CL_2 + HCl ambient. The growth rate for the 1.1 μm thick film was ≈ 0.35 μm/min., and the thickness uniformity across the 100 mm SEG wafers was ± 5%. The surface topography after selective epitaxial growth is shown in *Figure 2* . Dense areas of micron and submicron features exhibit excellent selectivity. The depth of the corner facet is significantly reduced due to the lower deposition pressure and the HCl flow used in this work. Further topography improvement was accomplished by CVD oxide deposition and etch-back planarization after the selective epitaxial growth which filled in the small corner facets. Subsequent processing steps followed a typical bulk silicon buried layer CMOS process. Due to the thin epitaxial layer, only 1 hour at 1050°C was necessary to obtain an n-well depth of 2 μm. The gate oxide thickness was 17 nm; shallow p+ and n+ junctions with sidewall spacers, titanium silicided sources, drains and gates, and refractory barrier metals were used under the aluminum metallization layer. *Table 1* provides a summary of process parameters.

ELECTRICAL MEASUREMENTS

One of the major yield-reducing factors in MOS processes is the quality of the thin gate oxide. Both bulk defects and LOCOS edge defects are encountered in conventional processes. Gate oxide integrity for the SEG process was found to be equal or superior to LOCOS type processes. The elimination of the silicon nitride deposition, selective oxidation and silicon nitride removal steps contribute to the improvement in gate oxide integrity. Breakdown field for the 17 nm oxide films is 12 MV/cm.

Excellent transistor characteristics were obtained. All transistors were fabricated with sources and drains butted against the thick oxide sidewalls. At threshold voltages of 0.66 V for n-channel and -0.56 V for p-channel transistors, long channel mobilities were 490 cm^2/Vs and 180 cm^2/Vs for n- and p- channels respectively. These values are identical with values obtained on a LOCOS buried-layer CMOS process, proof of the quality of the selectively-grown epitaxial film and consistent with the high channel doping levels required in submicron processes. *Figures 3 and 4* show transistor characteristics for minimum size devices available on our mask set.

One of the previously-reported device degradation phenomena, when using vertical oxide sidewalls for isolation in either SEG or trench processes, is the weak inversion along the sidewalls which affects n-channel transistors. *Figures 5 and 6* show subthreshold characteristics for short n- and p- channel transistors. No subthreshold "kink" in turn-off current is seen for these devices due to proper annealing, the <100> sidewall orientation, and the high doping level — approximately $1x10^{17}$ cm^{-3} in the channel. *Figures 7 and 8* compare the n-channel area and periphery reverse diode leakage of SEG and LOCOS buried-layer CMOS processes. Leakages for diodes built in the SEG material are only an order of magnitude higher than those for the conventional process. With process optimization, it is believed that even better results can be obtained.

The distance between n- and p-channel devices is an important factor in the density of submicron CMOS circuits. *Figure 9* shows latchup holding voltages of >12 V for n^+ to p^+ spacing of 2 μm, the minimum available on our mask set. Based on the structure used in this process, it is believed that spacings of 1 μm or less would also provide adequate latch-up protection.
High yielding ring oscillators were fabricated in this process. *Figure 10* shows ring oscillator speeds of 160 ps/stage at a supply voltage of 5 V.

SUMMARY

In conclusion, high quality SEG films with high selectivity were obtained and LOCOS quality p- and n-channel devices were made in these films. The shallow arsenic buried layers used in making p-channel transitors are ideal for high-performance bipolar transistors used in BiCMOS processes. The presence of the two independent buried layers allows for process optimization for latch-up suppression. This process circumvents the problems associated with LOCOS at submicron dimensions. The surface planarity and gate oxide integrity are excellent and the process is usable to 0.5 μm photolithographic features.

ACKNOWLEDGMENTS

The authors would like to thank M. Vora for his support and M. Brassington and M. El-Diwany for use of their test structures and software.

REFERENCES

1. Endo, N., et al, IEEE Transactions on Electron Devices, Vol ED-33, No.11, pp 1659-1666.

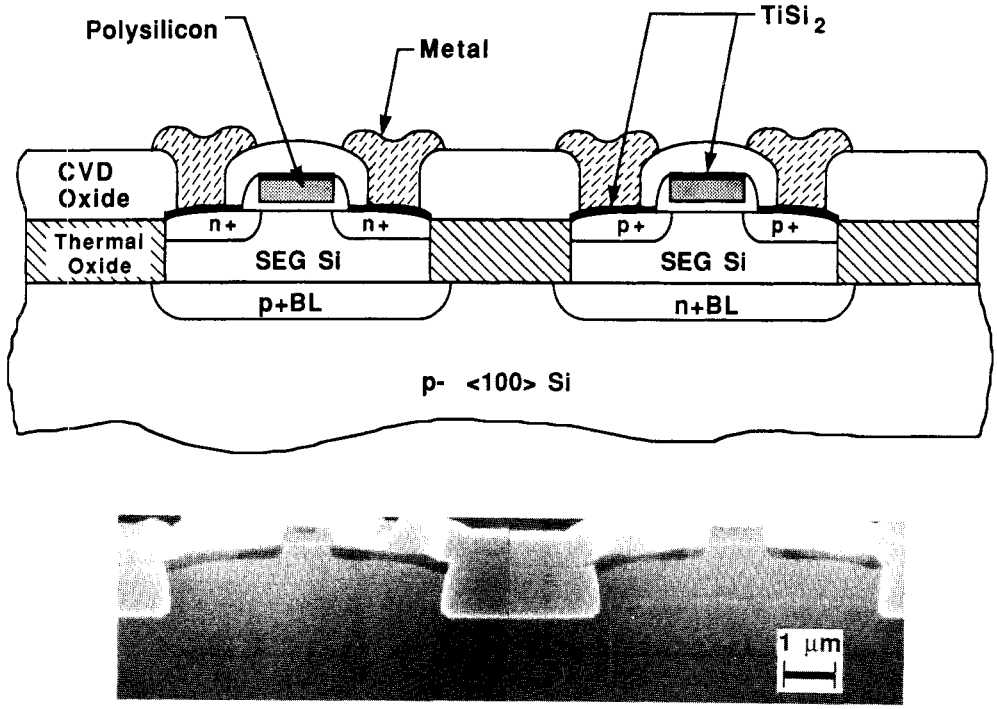

Figure 1. Process and SEM cross sections through a ring oscillator structure.

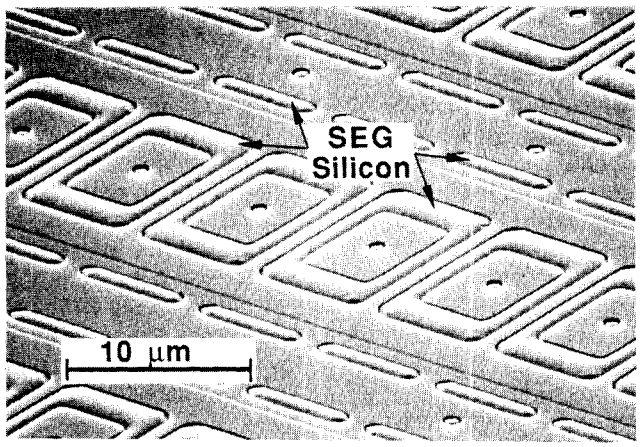

Figure 2. SEM photograph of memory test structure after selective epitaxial growth.

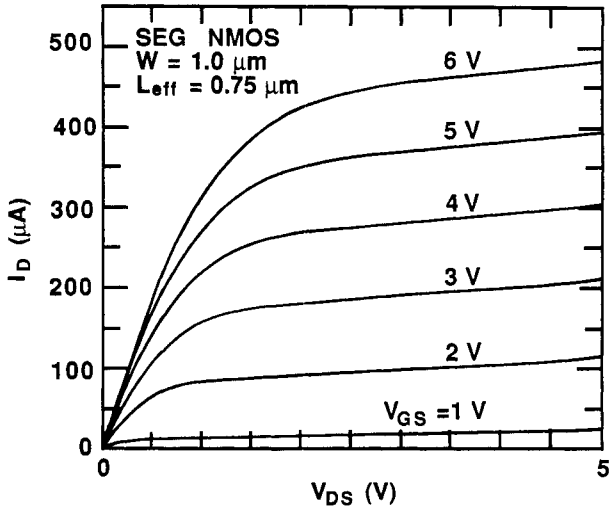

Figure 3. Small NMOS transistor characteristics in SEG silicon.

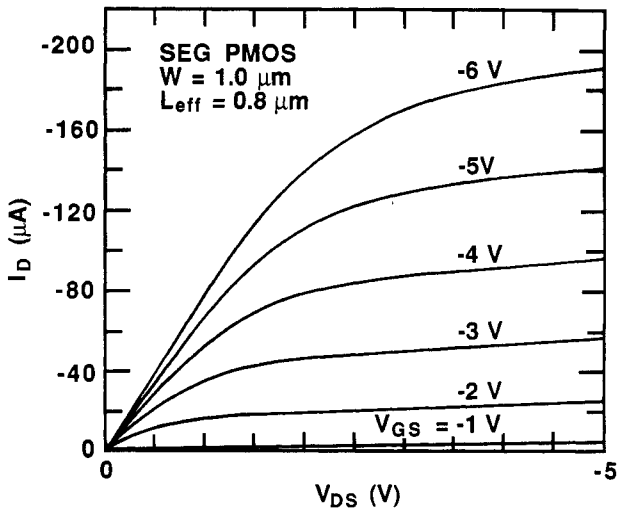

Figure 4. Small PMOS transistor characteristics in SEG silicon.

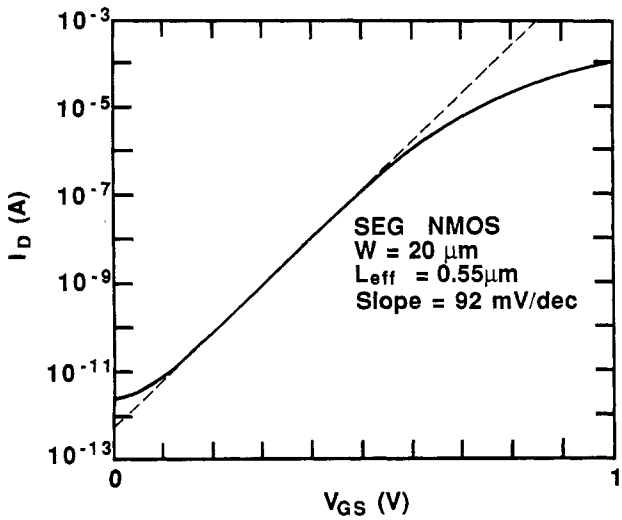

Figure 5. Subthreshold characteristic for n channel with SEG at V_{DS} = 0.1 V.

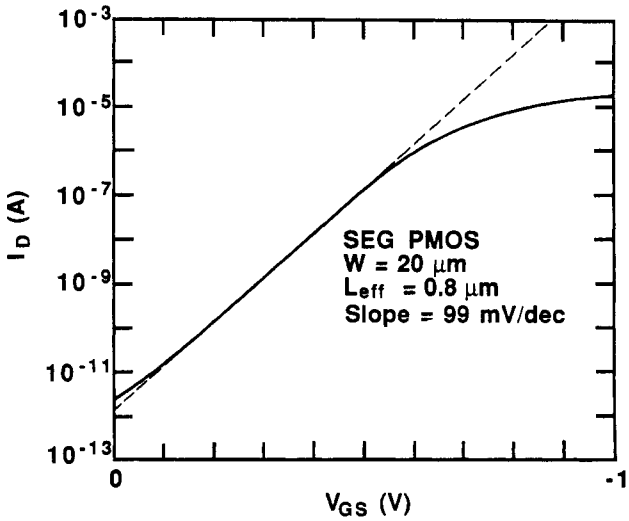

Figure 6. Subthreshold characteristic for p channel with SEG at V_{DS} = 0.1 V.

Table 1. Process Parameters for SEG CMOS

Parameter	Value
Field Oxide Thickness	1.1 μm
Selective Epi Layer Thickness	1.1 μm
Selective Epi Layer Concentration	$\approx 10^{15}$ #/cm^3
Gate Oxide Thickness	17 nm
n-well Depth	2 μm
n-well Resistance	20 Ω/sq
Silicided Poly Si, n+, p+ resistance	<5 Ω/sq
Junction Depth, n+ or p+	<0.3 μm

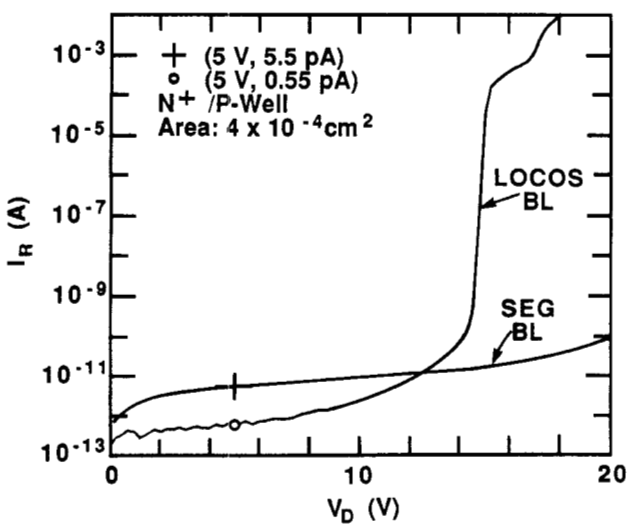

Figure 7. Area leakage for n+/p-well diodes of LOCOS and SEG buried layer CMOS processes.

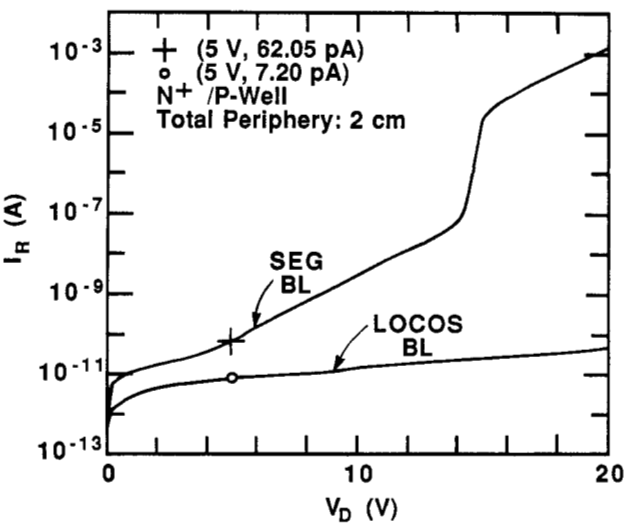

Figure 8. Peripheral leakage for n+/p-well diodes of LOCOS and SEG buried layer CMOS processes.

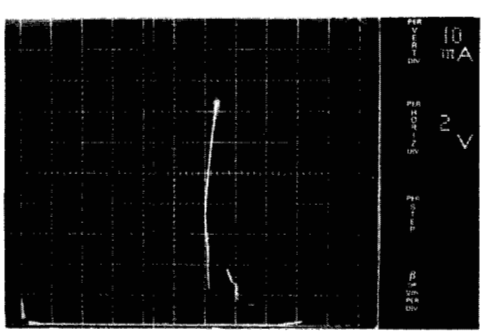

Figure 9. Latchup holding characteristic for SEG process with n+ to p+ spacing of 2 μm.

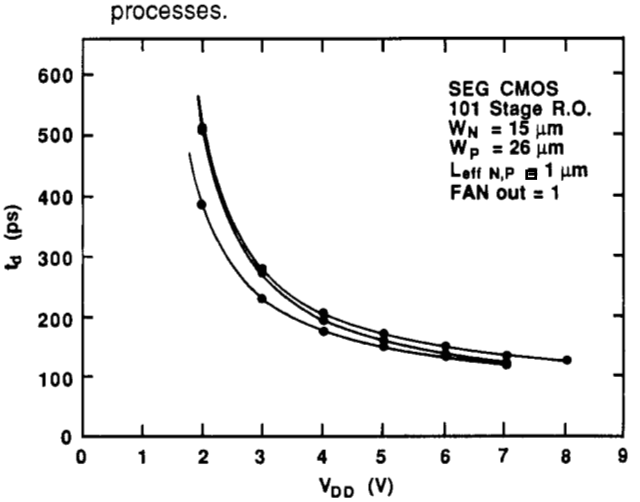

Figure 10. Ring oscillator gate delay for SEG CMOS.