Advanced CMOS Epitaxial Processing for Latch-Up Hardening and Improved Epilayer Quality

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Use of silicon epitaxial wafers for advanced CMOS device processing has led to improved latch-up hardening. However, the heavily doped substrates used to improve latch-up hardening can also degrade epilayer quality. Improvements in epilayers have been achieved through the application of both pre- and post-epitaxy intrinsic gettering that activates the growth of oxygen related precipitates. In p⁺ (100) and n⁺ (100) wafers, epilayer minority carrier lifetimes were improved by as much as three orders of magnitude.

WITH THE CONTINUED SCALING of device structures to the micron and submicron levels, use of silicon epitaxial wafers for advanced MOS technology is becoming widespread [1–5]. For NMOS, device fabrication with epi-wafers is an accepted process used by several IC manufacturers. For CMOS, the use of epitaxial structures is receiving more attention as increased latch-up prevention at minimal device geometries becomes necessary. This paper focuses on processing techniques for improving latch-up hardening that show why the use of epitaxial structures is attractive for CMOS processing. Basic concepts of intrinsic gettering, recent results on improved epilayer quality, and both pre-epitaxial and post-epitaxial gettering techniques applied to p⁺ and n⁺ epi-wafers are presented.

Latch-Up in CMOS Devices

Complimentary MOS (CMOS) circuits contain both p-channel and n-channel devices which are typically separated from each other by field oxide structures. Depending on the starting material used, these n- and p-channel devices can be located in either p-well or n-well structures. CMOS integrated circuits contain parasitic vertical and lateral pnp and npn transitors which can form a lateral pnpn circuit as shown in Fig. 1 for a n-well structure. Regenerative switching in this pnpn lateral current path causes latch-up which is one of the inherent limitations in CMOS device performance [6–9].

The holding current I_H (at which latch-up has occured) has been described by the following equation [6, 10]:

$$I_H = \frac{I_{Rw} \cdot B_L(B_V + 1) + I_{RS} \cdot B_V(B_L + 1)}{B_L \cdot B_V - 1}$$

where I_{Rw} = current through well, R_w = well resistance, I_{Rs} = current through the substrate, R_s = substrate resistance, B_L = parasitic lateral transistor current gain, B_V = parasitic vertical transistor current gain

Latch-up may be initiated when the product $B_V B_L$ is sufficient to allow regeneration. Since I_{Rw} is proportional to $1/R_w$, and I_{Rs} is proportional to $1/R_s$, in order to increase I_H and thereby improve latch-up resistance, B_V, B_L, R_w and R_s need to be decreased. Reducing R_s and R_w results in a need for larger lateral currents for latch-up initiation. Reducing B_V and B_L increases the latch-up threshold. Therefore, there are several CMOS processing alternatives for controlling and eliminating latch-up.

Techniques to Eliminate Latch-Up

Lifetime Reduction

Gold doping has been used to decrease the minority carrier lifetime and thereby reduce the current gain product of the parasitic vertical and lateral transistors in CMOS [10, 11]. However, control of this technique is difficult and can lead to increased device leakage current and degradation if improperly implemented. Improved latch-up hardening obtained through the use of intrinsic gettering of bulk oxygen precipitates to reduce lifetime has been reported for a p-well CMOS technology by Sakai, et al. [12], however, an n on n⁺ epi-wafer was significantly more effective.

Device Layout Techniques

Increased n-channel to p-channel spacing improves latch-up hardening [13, 14]. In addition, the use of guard ring structures can also improve latch-up hardening [14]. However, both of these techniques limit the ultimate obtainable device density.

Dielectric Isolation

Local oxidation of silicon (LOCOS) for partial dielectric isolation to separate the n-channel and p-channel devices will also improve CMOS latch-up hardening since it inhibits the formation of the lateral pnpn circuit caused by the combination of the vertical and lateral parasitic pnp and npn transistors as was shown in Fig. 1. However, the field oxide bird's beak encroachment makes LOCOS obsolete for device isolation distances less than 2 microns. At these distances isolation is possible by epitaxial trench isolation [15, 16] or selective epitaxy isolation [16, 17, 18, 19]. Complete dielectric isolation is posible by silicon on insulator (SOI) techniques where truly latch-up free CMOS devices are possible due to total isolation of the p-channel from n-channel region. Various SOI epitaxial techniques include: buried oxygen implantation (SIMOX) [21, 29], porous silicon oxidation (SOPS) [22, 23], and epitaxial lateral overgrowth (ELO) [24]. Although these techniques are subjects of extensive research at present, few if any have been used in production.

Well Profile Enhancement

Control of R_w, B_V and B_L can be achieved through tailoring the p-well or n-well profile to obtain the desired CMOS latch-up hardening. This can be accomplished through a deep-well or a retrogade-well. Results from a deep n-well CMOS process, where the standard n-well is 2 microns deep, and the deep n-well is 4 microns are shown in Fig. 2. The deep n-well R_w was half that of the standard n-well and B_V was also reduced by a factor of 2. However, B_L increased by a factor of 2 due to the increased lateral n-well diffusion. This effect is shown in Fig. 3. By resizing the n-well mask, the additional lateral diffusion can be corrected so as to maintain device real estate and reduce the beta product by a factor of 2.

A retrograde well profile can be formed by at least three techniques: (1) counter doping implantation; (2) high energy double implantation; (3) buried layer epitaxy. Each technique has its advantages and disadvantages.

Counter-doping retrograde profiles can be implemented by using a shallow implant to counter-dope the well through electrical compensation [25, 26]. Counter-doping presents a difficult problem in process control. For instance, stringent implant and processing control were required to obtain the n-well profile shown in Fig. 4. Also, mobility degradation is another concern with this technique.

Another technique to reproducibly obtain retrograde well structures is through high energy ion implantation [27]. A retrograde n-well profile obtained from a double phosphorous implantation at 200 keV and 1 MeV is shown in Fig. 5. Some of the limitations to this technique include cost and technical problems with mega-volt implantation. This may be overcome by doubly ionized implantations at lower energies.

A more viable approach to obtain retrograde wells is by use of buried layer epitaxial techniques, Fig. 6 [28]. Here, latch-up hardening improvements from an epitaxial structure are combined with a tailored well profile through the buried layer to control all four CMOS device parameters, R, R_w, B_V and B_L. Two key process concerns for this technique

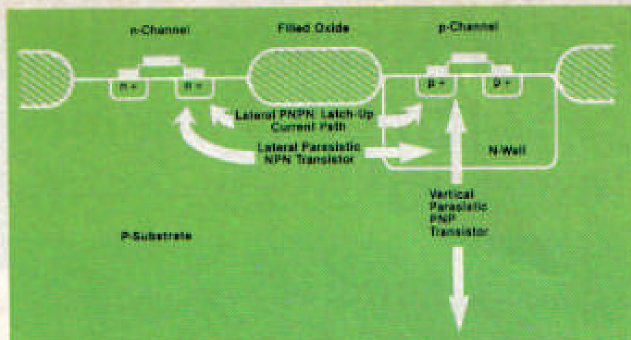

Fig. 1—Cross section of CMOS n-well structure showing latch-up.

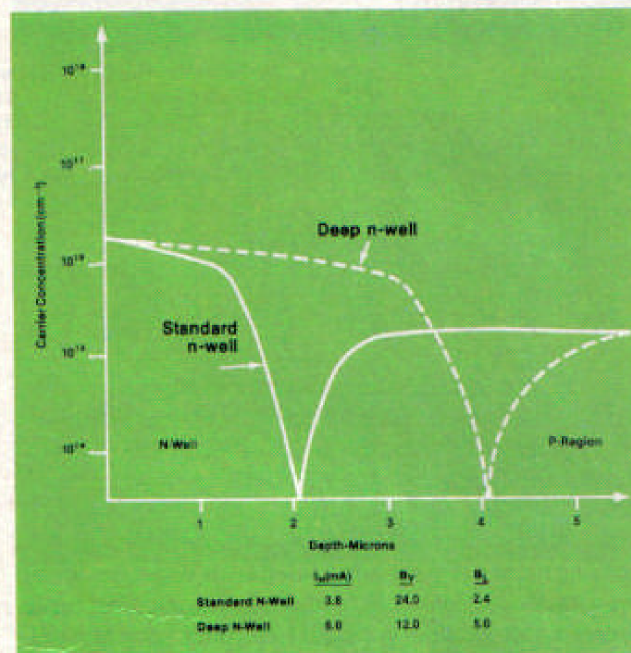

Fig. 2—2 micron standard n-well vs. 4 micron deep n-well CMOS processing results.

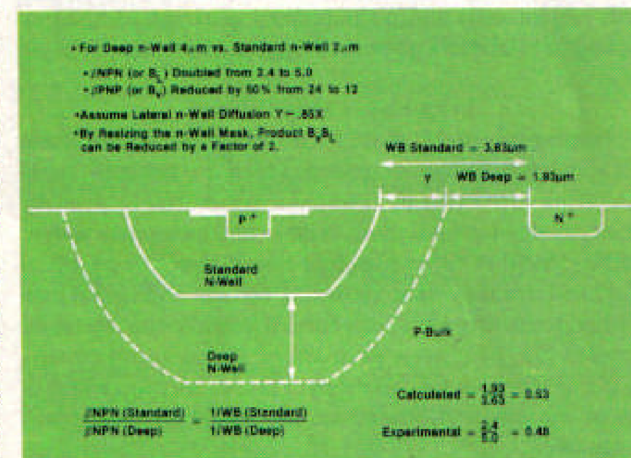

Fig. 3—Deep n-well CMOS process effects of increased lateral diffusion.

are: (1) Obtaining good pattern transfer of the alignment marks on (100) orientation; and (2) Minimizing autodoping and out-diffusion of the dopants in the heavily

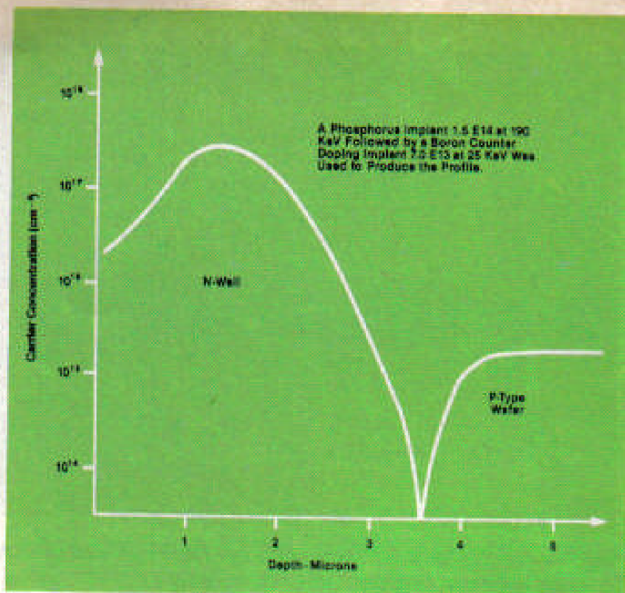

Fig. 4—Boron counter-doping technique for retrograde n-well formation.

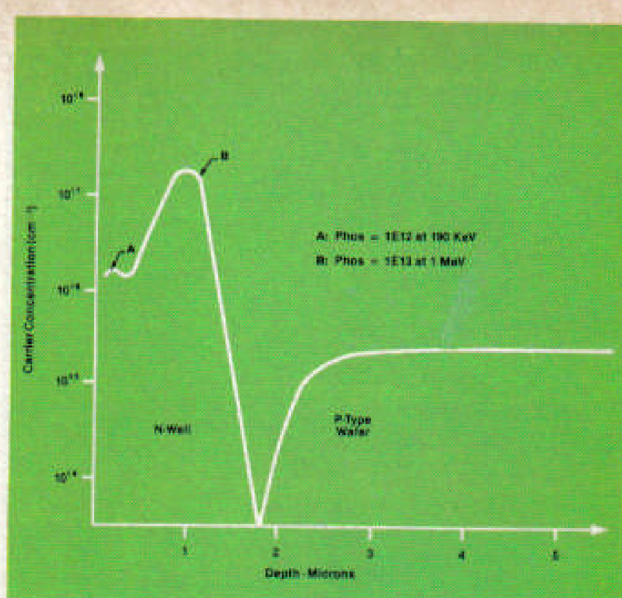

Fig. 5—Megavolt double phosphorus ion implantation for retrograde n-well formation.

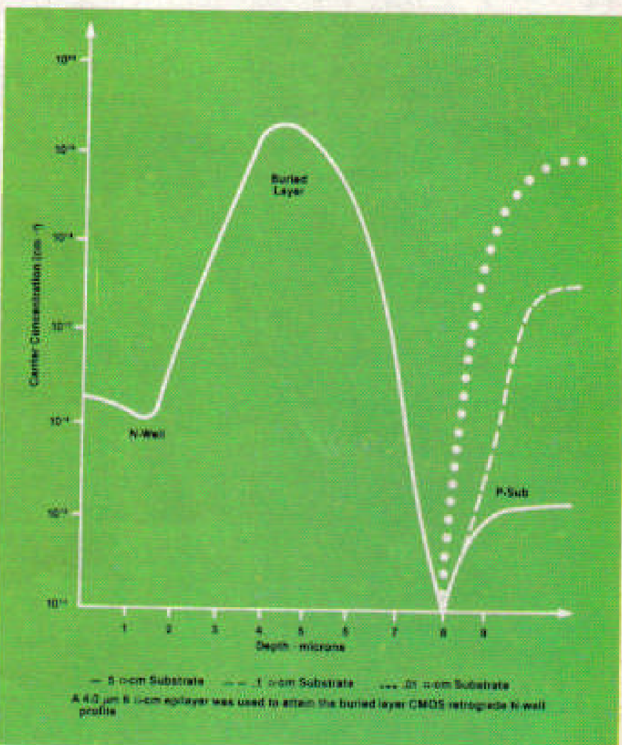

Fig. 6—Antimony buried layer epitaxial technique for retrograde n-well formation.

doped substrate and buried layer regions. Despite these limitations, buried layer epitaxy is the most promising technique for forming a retrograde well structure.

Epitaxial Structures

Reduction in the substrate resistance R_s obtained through use of epi-wafers (p-type epilayer over heavily doped p^+ substrates, or n-type epilayers over heavily doped n^+ substrates) has resulted in improved latch-up hardening [27, 29, 30, 31]. By tailoring the epi/substrate dopant transition region width and epilayer thickness to a given CMOS process, latch-up hardening can be optimized. Varying the distance from the bottom of the well to the epi/substrate transition region and the width of the epi/substrate transition region, not only affects R_s, but also the electric field induced by the high low junction formed at the epi/substrate transition region as shown in Figs. 7 and 8. Troutman, et al., [30] reported similar enhanced lateral current flow for an n-well CMOS epitaxial process. The enhanced current flow improved guard ring efficiency, thereby improving latch-up hardening. Similarly, Takacs, et al. [31], compared similar CMOS processes using p on p^+ epi-wafers and n on n^+ epi-wafers. They concluded that a sharper transition region improves latch-up hardness. Therefore, due to the rapid diffusion of p^+ boron dopant from the substrate into the epilayer compared to that of an n^+ antimony dopant, CMOS devices fabricated on n on n^+ epi-wafers are typically more latch-up resistive than are CMOS devices fabricated on p on p^+ epi-wafers.

Yamaguchi, et al. [16], have reported latch-up free CMOS devices at 0.5 μm geometry by using epitaxial structures combined with trench isolation techniques. Similar isolation can be obtained by selective epitaxy (SEG) as described by Endo, et al. [18].

To achieve maximum latch-up hardening, the epitaxial process must be tailored to each particular CMOS device process. By combining silicon epitaxial structures with well profile enhancement and advanced isolation techniques, device parameters can be tailored to achieve latch-up free devices even at sub-micron levels. However, one of the major concerns in using epitaxial layers for CMOS technology is the interaction between substrate defects and the epitaxial layer. This can lead to degradation of other CMOS device parameters such as epilayer lifetime, gate oxide integrity and junction leakage current. Therefore, various gettering techniques to control and eliminate these defects will be discussed in the following sections.

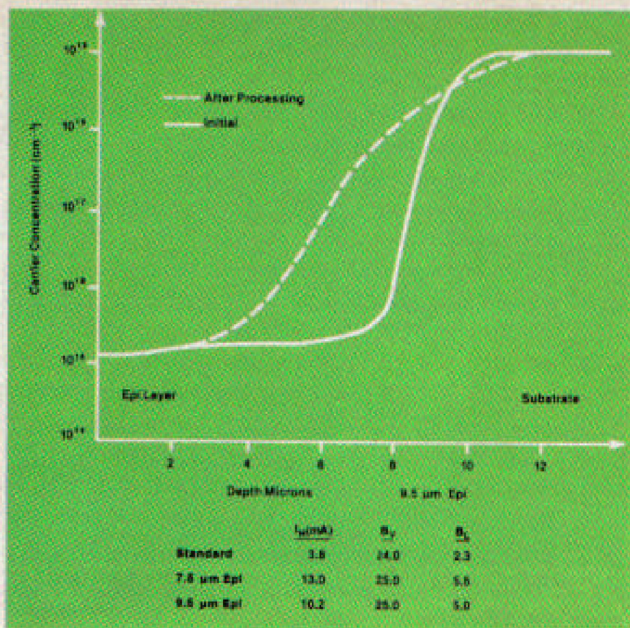

Fig. 7—p on p⁺ epitaxial structure for CMOS latch-up hardening.

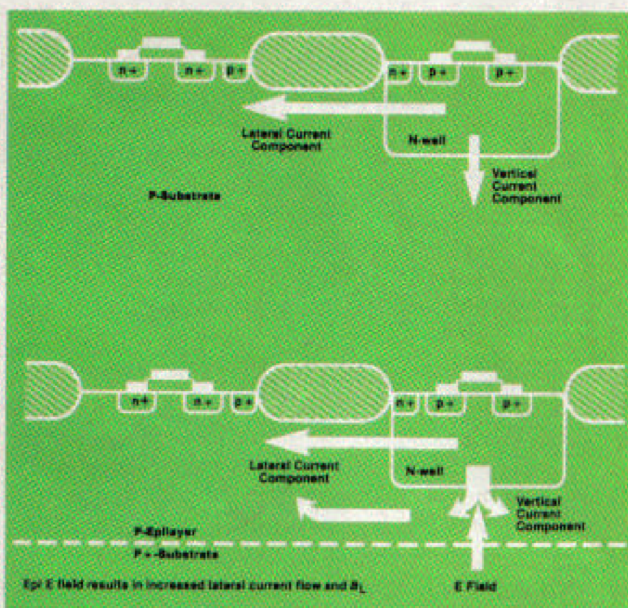

Fig. 8—p on p⁺ epitaxial structure induced electric field effects on latch-up hardening.

Gettering in Silicon

During silicon device fabrication, a wafer is subjected to numerous conditions which can lead to process induced defects and contamination. If these defects or impurities are located in the active regions, they can hinder device performance and lower yield. However, if the imperfections (defects) are located in an inactive region, good device performance can be achieved.

Instrinsic gettering in silicon can be used to remove metallic impurities and other defects from the near surface (active device) region by trapping them in the bulk of the wafer [32, 33]; see Fig. 9. In intrinsic gettering (IG), the intrinsic mate-

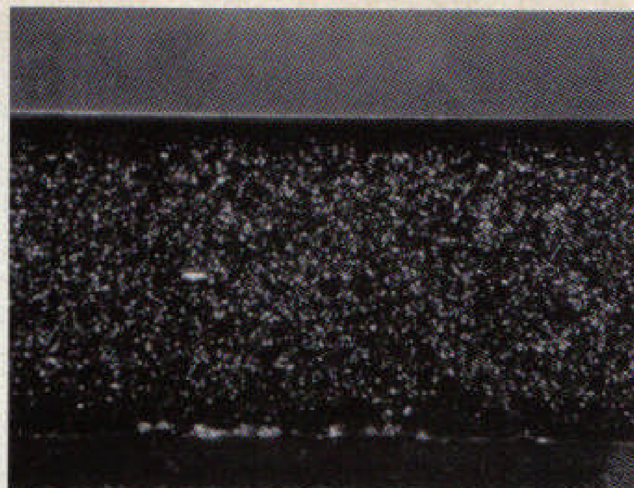

Fig. 9—Intrinsic gettered wafer showing (110) cross section with denuded zone and bulk intrinsic gettering sites.

rial properties of the silicon wafer (oxygen, carbon, silicon-vacancies, silicon-interstitials, dopant point defects) are used to induce the formation of SiO_x complexes (oxygen precipitation). These SiO_x precipitates generate lattice disorder and dislocations which act as gettering sites [34, 35].

Intrinsic gettering techniques applied to bulk silicon wafers have been reported to improve NMOS and CMOS device performance and yields [36, 37]. Their application to silicon epitaxial processing is extremely limited and has been described mainly for bipolar devices using an n on p epitaxial structure [38, 39, 40, 41]. For CMOS technology where heavily doped n⁺ and p⁺ (100) orientation epitaxial substrates are used, the interaction of boron, phosphorus, arsenic, or antimony doping at concentrations $>5\times10^{18}$ atoms/cm³, with the oxygen precipitation gettering mechanism is not fully understood. The application of IG concepts to CMOS epitaxial processing will be discussed in the following sections.

Denuded Zone Formation

For effective IG, both a denuded zone in the device active region and gettering sites in the bulk of the wafer, must be formed; see Fig. 9. The denuded zone can be created by subjecting the wafer to a "denudation process" which causes oxygen atoms to out-diffuse from the wafer surface resulting in a region depleted of oxygen. Figure 10 shows an oxygen profile in the denuded zone region of an IG wafer measured by Secondary Ion Mass-Spectroscopy (SIMS). Furnace anneals at temperatures above 1100 °C in ambients of argon, oxygen, nitrogen, or their combinations are very effective for denuding [34]. A protective capping oxide is recommended for pevention of surface nitridation and pitting. An oxidizing ambient for denudation is not recommended by the authors because of the oxygen induced surface stacking faults (OISF) that can form on the wafer surface at temperatures above 1100 °C; see Fig. 11. Once a denuded zone has been formed, oxygen precipitation in the bulk of the wafer is induced. From a precipitation matrix study, the optimum temperature for oxygen precipitation

was determined to be 950 °C for one set of wafers [43], and results from an earlier study [41, 42] showed that the oxygen precipitation rate at 950 °C can be enhanced by a 700 °C anneal. The anneal is very effective in nucleating SiO_x precipitate sites. A modified three-step IG thermal cycle is shown in Fig. 12. It is composed of: (1) denudation, (2) SiO_x precipitate nucleation, and (3) SiO_x precipitation and growth. More detail on the evolution and impact of each heat treatment on the silicon wafer material properties can be found in refs. 34, 35, and 42.

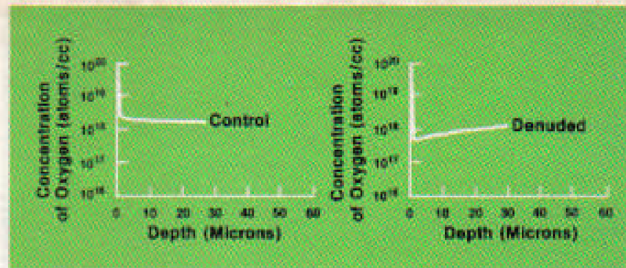

Fig. 10—SIMS analysis showing oxygen depletion in the denuded zone.

CMOS Epitaxial Intrinsic Gettering Techniques

Intrinsic gettering techniques in heavily doped wafers have been investigated by various authors. Rozgonyi and Pearce [44] have observed oxygen precipitation in wafers with high doping concentrations of boron, arsenic and antimony. Tsuya et al. [45] have reported micro-defect formation in heavily doped n-type wafers after anneals of up to 72 hours at various temperatures. Gupta, et al. [46], have reported improved device performance and yields in silicon gate MOS structures by applying a three-step pre-epitaxial IG process to n^+ wafers. Borland, et al. [47, 48], used various pre-epitaxial IG cycles on p on p^+ and n on n^+ epitaxial processes to improve epilayer lifetime. Dyson et al. [49, 50] have also reported extremely high lifetime p on p^+ and n on n^+ getter enhanced epi-wafers.

Epitaxial intrinsic gettering techniques can be divided into two distinct groups: (1) pre-epitaxial gettering, (2) post-epitaxial gettering. These gettering techniques can be used to activate the intrinsic gettering mechanism in the substrate wafer either prior to or after CVD epitaxial growth. The modified three-step IG cycle shown in Fig. 12 is an example of a pre-epitaxial IG process. Uniform high quality silicon epitaxial layers can be achieved through pre-epitaxial gettering. Figure 13 compares a non-gettered p on p^+ epi-wafer to a three-step IG p on p^+ epi-wafer from the same silicon supplier. A denuded zone 17 microns deep with bulk intrinsic gettering sites was formed in the IG epi-wafer. The pre-epitaxial IG technique improved the epilayer lifetime by over two orders of magnitude. Although this technique is very effective for gettering, it has the disavantages of adding additional processing and cleaning steps to the substrate wafer prior to epi deposition. This would increase the cost of the epi-wafer and would have to be done by the silicon epitaxial supplier. Another approach that will keep the cost of the epi-wafer down, is post-epitaxial gettering which could be done by the integrated circuit manufacturer rather than by the epitaxial producer.

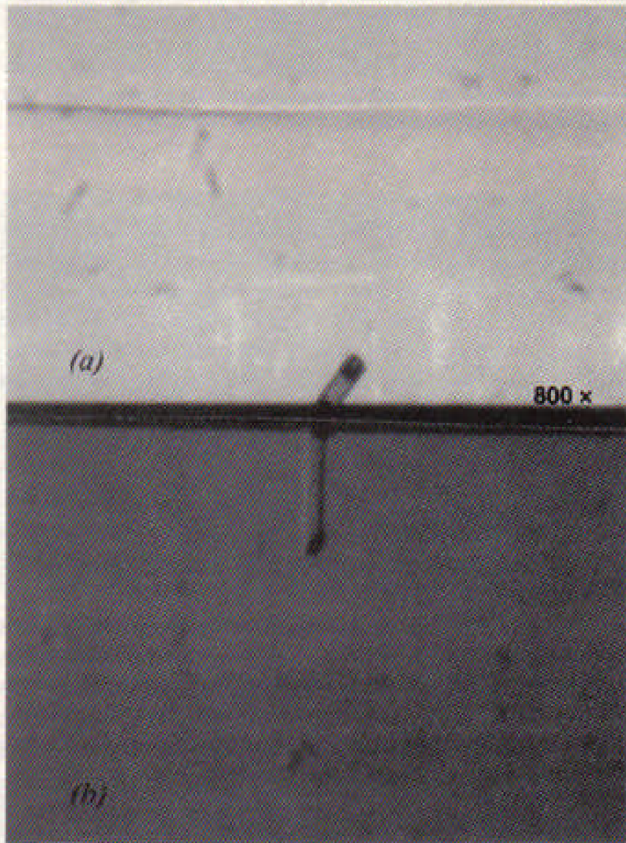

Fig. 11—Wright etch defect delineated on (a) (100) surface, and (b) (110) cross section; defect analysis of oxygen induced surface stacking fault (OISF) by an oxidizing denudation ambient anneal.

Post-epitaxial gettering can be achieved through three means: (1) process induced gettering, (2) enhanced process induced gettering, or (3) pre-processing induced gettering. Process induced gettering can be inherent in some CMOS fabrication. For example, an n-well or p-well drive-in process at temperatures above 1100 °C is effective not only for ion implantation damage annealing, carrier activation, and diffusion, but is also an effective denudation process for oxygen. Oxygen precipation and growth in the bulk of the wafer occur during the field oxidation process at temperatures between 900 °C to 1000 °C. Therefore, process in-

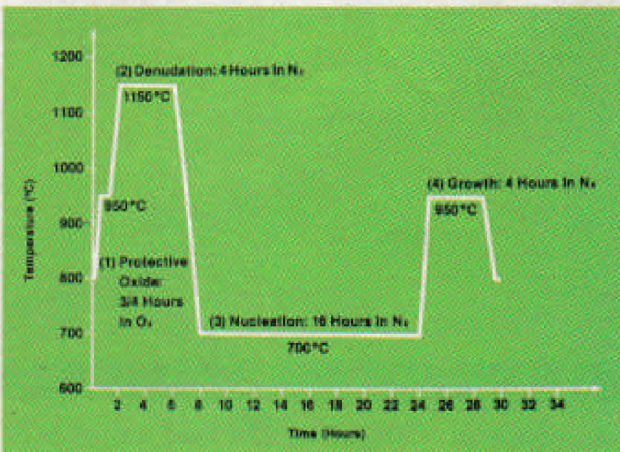

Fig. 12—Modified three-step intrinsic gettering cycle.

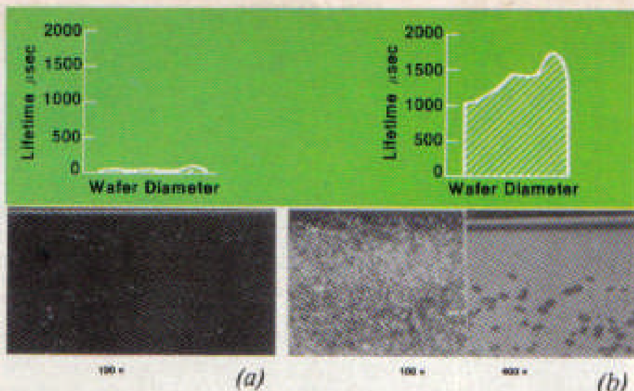

Fig. 13—(a) Standard epi vs. (b) three-step I.G. p on p⁺ 0.01 ohm-cm epi-wafer, showing MOS capacitance-time lifetime and (110) cross-sectional defect analysis.

duced gettering can occur innately in some CMOS processes. Figure 14 shows an example of process induced gettering in p on p⁺ epi-wafers subjectd to an n-well CMOS VLSI process. Note the improvement in lifetime at the end of the process and bulk micro-defects in the (110) cross-sectional analysis. Other CMOS processes may require an enhanced process induced gettering technique shown in Fig. 15. Enhanced gettering is achieved by adding a 16 hour 700 °C nucleation step between the well drive-in and the field oxidation processing steps. This will increase the density of SiO_x precipitates formed during the field oxidation process. It also increases the density of available gettering sites during the critical gate oxidation process.

If neither of these two post-epitaxial gettering techniques is effective enough, then a third technique called pre-processing induced gettering can be used; see Fig. 16. In this technique, intrinsic gettering is activated in the substrate wafer prior to CMOS device processing by subjecting the epi-wafer to an SiO_x nucleation and precipitate growth cycle. In summary, depending on the particular CMOS process flow being used, four different epitaxial gettering techniques are available to ensure an excellent quality silicon epitaxial layer for device fabrication.

P on P⁺ Epitaxial Structures

A typical CMOS p on p⁺ epi-wafer will have an epilayer of 10 ohm-cm, 15 to 20 µm thick, grown at 1130 °C, using $SiHCl_3$ as the gas source. The p⁺ substrate wafers are heavily boron doped (~ $10^{19}/cm^3$), 0.01 ohm-cm, (100) orienta-

Fig. 15—CMOS process flow to achieve enhanced-process induced gettering.

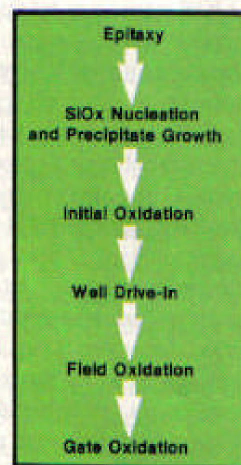

Fig. 16—CMOS process flow to achieve pre-processing induced gettering.

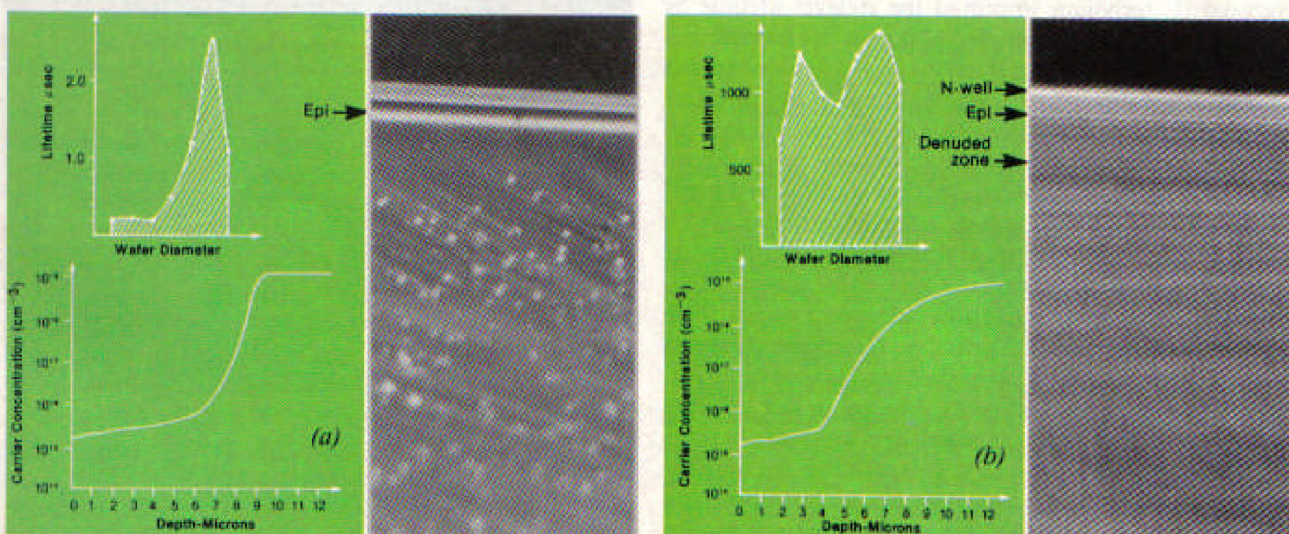

Fig. 14—Process induced intrinsic gettering in p on p⁺ epi-wafer from an n-well CMOS process flow. (a) After initial oxidation; (b) After gate oxidation.

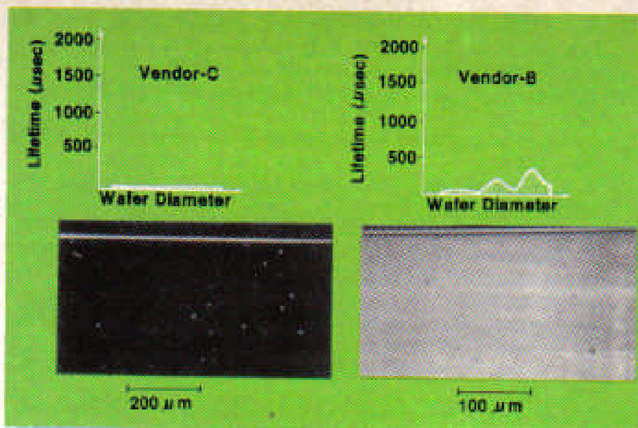

Fig. 17—Impact of as-grown (standard epi-wafer) SiO_x precipitates in p^+ substrates on p epilayer lifetime.

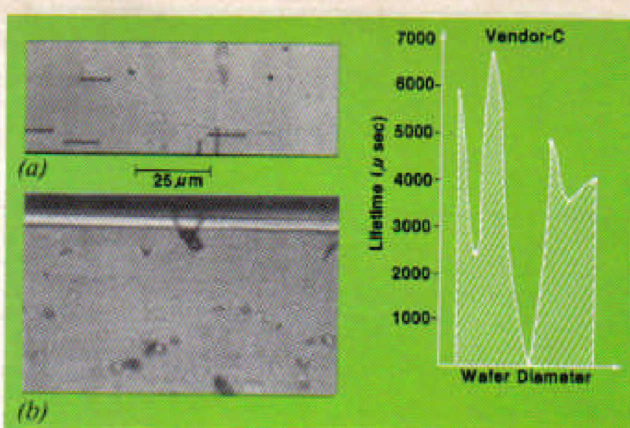

Fig. 18—Impact of p^+ substrate surface stacking fault on p epitaxial induced stacking fault. (a) (100) surface; (b) (110) cross section.

tion, and depending on the silicon substrate wafer thermal history, as-grown SiO_x precipitates can be present in the substrate wafer. These micro-defects are induced during the silicon ingot crystal growth and cool down process. They enhance process induced gettering. Two non-gettered p on p^+ epi-wafers from different silicon vendors are shown in Fig. 17. The (110) cross-sectional defect analysis revealed as-grown precipitates in the epi-wafer substrate from vendor B. Regions with bulk precipitates had high epilayer lifetimes. However, if a micro-defect is located at the substrate wafer surface, it can be transmitted through the epilayer giving rise to epitaxial stacking faults which can degrade the epilayer lifetime, see Fig. 18.

In summary, p on p^+ epitaxial intrinsic gettering techniques improved the epilayer lifetime by over three orders of magnitude. Therefore, p-type epilayer lifetimes as high as p-bulk IG wafer lifetimes can be achieved through the proper epitaxial gettering technique as shown in Fig. 19.

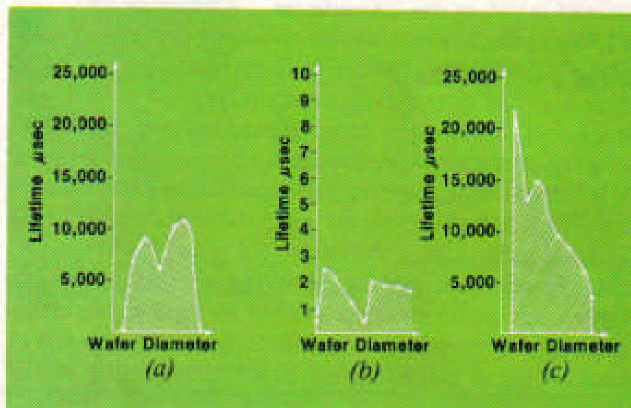

Fig. 19—Summary of MOS capacitance-time minority carrier lifetimes measured on 6 ohm-cm p (100) material comparing (a) best bulk wafer, to p/p^+ epi-wafers; (b) standard; and (c) best IG.

N on N⁺ Epitaxial Structures

N-type epilayers used for n on n^+ epi-wafers are thinner than p-type epilayers on p on p^+ epi-wafers because of the slower diffusion rate of antimony in heavily doped n^+ substrate wafers in contrast to boron. The epilayers are usually 10 μm thick. Heavily doped antimony wafers are more resistive to oxygen precipitate and micro-defect for mation than are n^-, p^- and p^+ wafers. This phenomenon is not totally understood although it is due partially to the significant reduction of the oxygen present in the n^+ wafers. The oxygen content has been reported to be two times lower in n^+ wafers than that typically found in p^-, n^- and p^+ Cz-grown wafers [51, 52]. Therefore, n-type epilayers are inherently inferior in quality compared to p-type epilayers and a high density ($> 10^5/cm^2$) of epi-surface shallow etch pits are consistently observed in non-gettered n-type epilayers. In addition, epilayer lifetimes are usually less than 10 μsec; see Fig. 20. Because of the difficulty of oxygen precipitate formation, a prolonged 950 °C anneal is required to form a well defined denuded zone with bulk intrinsic gettering sites in n^+ wafers; see Fig. 21 [48]. By using extended anneals (24 to 100 hours), n-type epilayer lifetime as high as

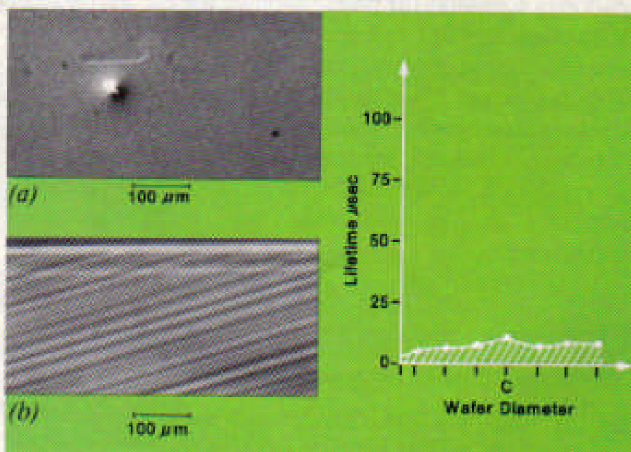

Fig. 20—Standard n on n^+ epi-wafer (non gettered). (a) (100) surface; (b) (110) cross section.

3.1 msec has been achieved on IG n^+ substrates. This represents an improvement in lifetime by over two and a half orders of magnitude.

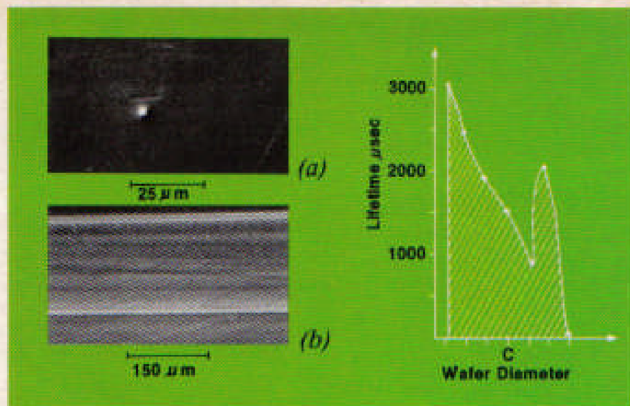

Fig. 21—Intrinsically gettered n on n⁺ epi-wafer. (a) (100) surface; (b) (110) cross section.

Conclusion

Using epitaxial structures for advanced CMOS technology can provide very effective latch-up hardening in CMOS devices. A key issue is the interaction between intrinsic gettering and the heavily doped substrates used in CMOS epitaxial processing. Improved silicon epitaxial layers can be achieved through applying pre-epitaxial or post-epitaxial intrinsic gettering techniques to the substrate wafer. These gettering techniques are effective for p on p^+ and n on n^+ CMOS epitaxial processing. N^+ wafers are very resistive to oxygen precipitate and micro-defect formation. Nevertheless, improvements in epilayer MOS lifetime by as much as three orders of magnitude are possible depending on the resistivity of the substrate. Through the proper epitaxial gettering technique, improved CMOS device performance and yields have been achieved.

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